Course Work – 01

Seminar on Analog IC Design

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CERTIFICATE

This is to certify that the report entitled "Analog IC Design" submitted by Mr.Guruprasad (Reg No. 140900006) is a bonafide report of the research course work carried out by him, and it is accepted as the "course work – 01" in partial fulfillment of the requirement for the award of the degree of Doctor of Philosophy.

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1. Integrated Circuit Devices and Modelling

In this chapter, both the operation and modelling of semiconductor devices are described.

1.1 MOS Transistors

Presently, the most popular technology for realizing microcircuits makes use of MOS transistors. MOS circuits normally use two complementary types of transistors—n-channel and p-channel. While n-channel devices conduct with a positive gate voltage, p-channel devices conduct with a negative gate voltage. Moreover, electrons are used to conduct current in n-channel transistors, while holes are used in p-channel transistors. Microcircuits containing both n-channel and p-channel transistors are called CMOS circuits [Complementary Metal Oxide Semiconductor]. Before CMOS technology became widely available, most MOS processes made use of only n-channel transistors (NMOS). However, often two different types of n-channel transistors could be realized. One type is enhancement n-channel transistors which is similar to the n-channel transistors realized in CMOS technologies. Enhancement transistors require a positive gate-to-source voltage to conduct current. The other type is depletion transistors which conduct current with a gate-source voltage of 0V. Depletion transistors are used to create high impedance loads in NMOS logic gates.

A typical cross section of an n-channel enhancement-type MOS transistor is shown in Figure 1.1 with no voltage applied to the gate, the n^+ source and drain regions are separated by the p^- substrate. The distance between the drain and the source is called the channel length. In present MOS technologies, the minimum channel length may be as small as 28 nm. The source terminal of an n-channel transistor is defined as whichever of the two terminals has a lower voltage. For a p-channel transistor, the source would be the terminal with the higher voltage. When a transistor is turned on, current flows from the drain to the source in an n-channel transistor and from the source to the drain in a p-channel transistor. In both cases, the true carriers travel from the source to drain, but the current directions are different because n-channel carriers (electrons) are negative, whereas p-channel carriers (holes) are positive.

The gate is normally realized using polysilicon, which is heavily doped non-crystalline (or amorphous) silicon. Polysilicon gates are used (instead of metal) because polysilicon has allowed the dimensions of the transistor to be realized much more accurately during the patterning of the transistor. This higher geometric accuracy has resulted in smaller, faster transistors. However, due to the relatively higher resistance of polysilicon, there are continuous efforts to realize metal gates in CMOS fabrication technologies.

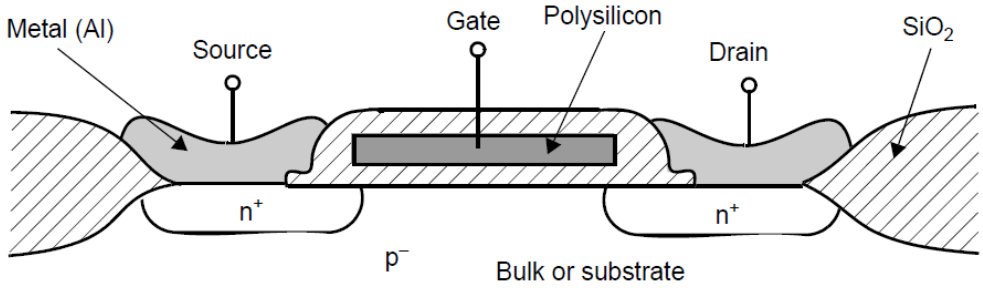


Figure 1.1 Enhancement MOS structure

The gate is physically separated from the surface of the silicon by a thin insulator made of silicon dioxide (SiO_2). Thus, the gate is electrically isolated from the channel and affects the channel (and hence, the transistor current) only through electrostatic (capacitive) coupling. The typical thickness of the SiO_2 insulator between the gate and the channel is presently between 1 to 30 nm. Since the gate is electrically isolated from the channel, it does not conduct appreciable dc current. However, because of the inherent capacitances in MOS transistors, transient gate currents do exist when gate voltage is quickly changing. Normally the p^- substrate (or bulk) is connected to the most negative voltage in a microcircuit. In analog circuits, this might be the negative power supply and in digital circuits it is normally ground or 0V. This connection results in all transistors placed in the substrate being surrounded by reverse-biased junctions, which electrically isolate the transistors and thereby prevent conduction between the transistor terminals and the substrate (unless, of course, they are connected together through some other means).[1]

Basic operation

For small positive gate voltages, the positive carriers in the channel under the gate are initially repulsed and the channel changes from a p^- doping level to a depletion region. As a more positive gate voltage is applied, the gate attracts negative charge from the source and drain regions, and the channel becomes an n region with mobile electrons connecting the drain and source regions. In short, a sufficiently large positive gate-source voltage changes the channel beneath the gate to an n region, and the channel is said to be inverted.

The gate-source voltage, for which the concentration of electrons under the gate is equal to the concentration of holes in the p^- substrate far from the gate, is commonly referred to as the transistor threshold voltage and denoted V_{tn} (for n-channel transistors). For gate-source voltages larger than V_{tn}, there is an n-type channel present, and conduction between the drain and the source can occur. For gate-source voltages less than V_{tn}, it is normally assumed that the transistor is off and no current flows between the drain and the source. However, it should be noted that this assumption of zero drain-source current for a transistor that is off is only an approximation. In fact, for gate voltages around V_{tn}, there is no abrupt current change, and for gate-source voltages slightly less than V_{tn}, small amounts of subthreshold current can flow.

When the gate-source voltage, V_{GS}, is larger than V_{tn}, the channel is present. As V_{GS} is increased, the density of electrons in the channel increases. Indeed, the carrier density, and therefore the charge density, is proportional to V_{GS}-V_{tn}, which is often called the effective gate-source voltage and denoted as V_{eff}.

$$V_{eff} = V_{GS} - V_{tn} \qquad 1.1$$

MOSFET operation regions are shown in the Figure 1.2. In that it is shown that if the drain voltage is increased above 0V, a drain-source potential difference exists. This difference results in current flowing from the drain to the source. The relationship between V_{DS} and the drain-source current, I_D, is the same as for a resistor, assuming V_{DS} is small. This relationship is given by

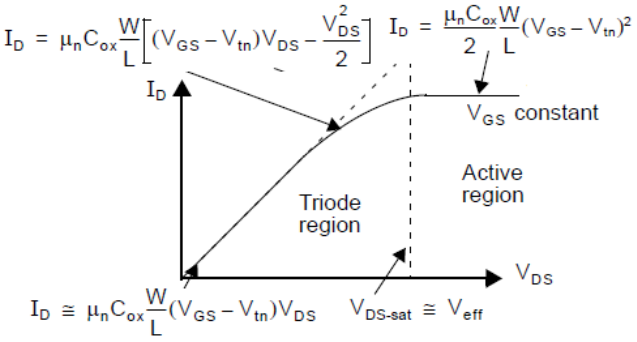


Figure 1.2 MOSFET operation regions [1]

$$I_D = \mu_n C_{ox} V_{eff} V_{DS} W/L \quad (1.2)$$

μ_n the mobility of electrons near the silicon surface,

$$C_{ox} = \frac{K_{ox}\varepsilon_0}{t_{ox}} \quad (1.3)$$

K_{ox} – relative permittivity of SiO_2, t_{ox} – Oxide thickness under gate , W is the width of the channel and L is the length of the channel.

Near V_{tn}, I_D varies with V_{DS} as given by the equation

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[V_{eff} V_{DS} - \frac{{V_{DS}}^2}{2}\right] \quad (1.4)$$

When $V_{DS} > V_{tn}$, I_D is almost independent of V_{DS} given by equation

$$I_D = \frac{\mu_n C_{ox} W}{2L} {V_{eff}}^2 \quad (1.5)$$

1.2 Channel-length modulation

The drain current, I_D, is independent of the drain-source voltage. This independence is only true to a first-order approximation. The major source of error is due to the channel length shrinking as V_{DS} increases. A pinched-off region with very little charge exists between the drain and the channel. The voltage at the end of the channel closest to the drain is fixed at V_{eff}. The voltage difference between the drain and the near end of the channel lies across a short depletion region often called the pinch-off region. As V_{DS} becomes larger than, this depletion region surrounding the drain junction increases its width in a square-root relationship with respect to V_{DS}. This increase in the width of the depletion region surrounding the drain junction decreases the effective channel length. In turn, this decrease in effective channel length increases the drain current, resulting in what is commonly referred to as channel-length modulation as shown in Figure 1.3.

The expression for I_D considering channel length modulation is given by equation

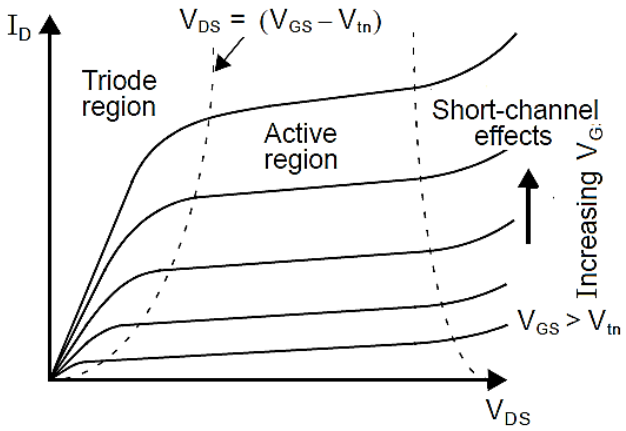


Figure 1.3 MOSFET output characteristics

$$I_D = \frac{\mu_n C_{ox} W}{2L} V_{eff}{}^2 [1 + \lambda (V_{DS} - V_{eff})^2] \quad 1.6$$

where λ is the output impedance constant given by

$$\lambda = \frac{k_{ds}}{2L\sqrt{V_{DS} - V_{eff} + \phi_0}} \quad 1.7$$

1.3 Body Effect

The large-signal equations in the preceding section were based on the assumption that the source voltage was same as the body voltage (i.e., the substrate or bulk voltage of a NMOS device). However, often the source and body can be at different voltages. Hence, the amount of charge in the channel and conduction through it is influenced by the potential difference between body and source. The body effect is the influence of the body potential on the channel, modelled as an increase in the threshold voltage, V_{tn}, with increasing source-to body reverse-bias.[1]

$$V_{tn} = V_{tn0} + \Upsilon(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}) \quad 1.8$$

V_{tn0}- threshold with zero V_{SB}

ϕ_F –fermi potential of the body $\phi_F = kT/q \ln (N_A/n_i)$

Υ- Body effect constant $\Upsilon = \frac{\sqrt{2qN_A K_S \varepsilon_0}}{C_{ox}}$

1.4 Low-Frequency Small-Signal Modelling in the Active Region

The most commonly used low-frequency small-signal model for a MOS transistor operating in the active region is shown in Figure 1.4.

Transconductance g_m is given by

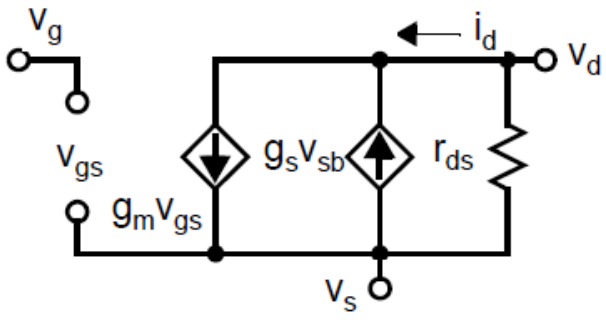


Figure 1.4 Low frequency small signal mode

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{1.9}$$

$$g_m = \frac{\mu_n C_{ox} W V_{eff}}{L} \tag{1.10}$$

The second voltage-controlled current-source g_s is given by

$$g_s = \frac{\partial I_D}{\partial V_{SB}} \tag{1.11}$$

$$g_s = \frac{g_m \Upsilon}{2\sqrt{V_{SB}+|\phi_F|}} \tag{1.12}$$

Output impedance r_{ds} is given by

$$r_{ds} = \frac{1}{\lambda I_D} \tag{1.13}$$

1.5 High-Frequency Small-Signal Modelling in the Active Region

A high-frequency model of a MOSFET in the active region is shown in Figure 1.5. Most of the capacitors in the small-signal model are related to the physical transistor.The largest capacitor C_{gs} is primarily due to the change in channel charge as a result of a change in V_{GS}. It can be shown that, it is approximately given by

$$C_{gs} = \tfrac{2}{3} WLC_{ox} \tag{1.14}$$

The source-bulk capacitance, C_{sb}, is given by

$$C_{sb} = C'_{sb} + C_{s\text{-}sw} \qquad C'_{sb} = \frac{(A_{ch}+A_s)C_{j0}}{\sqrt{1+\frac{V_{SB}}{\phi_0}}} \tag{1.15}$$

where A_s is the area of the source junction, A_{ch} is the area of the channel, $C_{s\text{-}sw}$ is source side wall capacitance

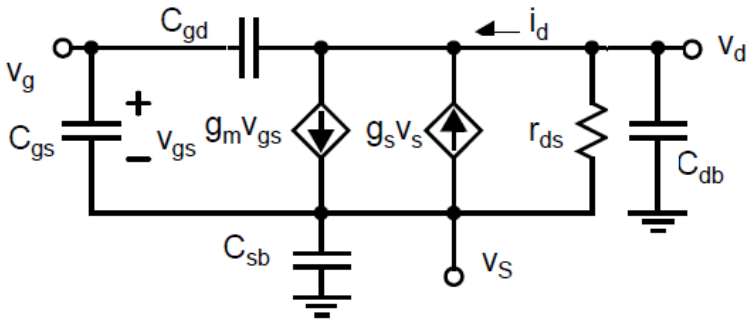


Figure 1.5 High Frequency Small signal Model

drain-bulk capacitance, C_{db} , given by

$C_{db} = C'_{db} + C_{d\text{-}sw}$

$$C'_{db} = \frac{(A_d)C_{j0}}{\sqrt{1+\frac{V_{DB}}{\phi_0}}} \qquad 1.15$$

A_d is the area of the drain junction; $C_{d\text{-}sw}$ is the drain side wall capacitance

The capacitance C_{gd}, is called the Miller capacitance and given by

$$C_{gd} = C_{ox}WL_{ov} \qquad 1.16$$

1.6 Small-Signal Modelling in the Triode and Cut off Regions

The low-frequency, small-signal model of a MOS transistor in the triode region is a voltage-controlled resistor with V_{GS} used as the control terminal. The accurate small-signal modelling of the high-frequency operation of a transistor in the triode region is nontrivial (even with the use of a computer simulation). A moderately accurate model is shown in Figure 1.6

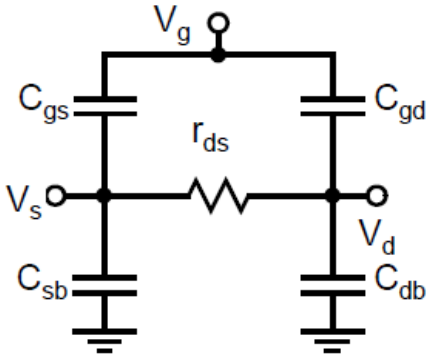


Figure 1.6 Small Signal Model in triode region

1.7 Advanced MOS Modelling

The square-law relationship between effective gate-source voltage and drain current expressed in the equation is only valid for active operation in strong inversion. For very small (and negative) values of V_{eff} , MOS devices operate in weak inversion, also called subthreshold operation, where an exponential voltage-current relationship holds. For large values of V_{eff}, a combination of effects gives rise to a sub-square-law voltage–current relationship.[1]

1.7.1 Subthreshold Operation

The device equations presented for active or triode region of MOS transistors in the preceding sections are all based on the assumption that V_{eff}, is greater than about 100mV and the device is in strong inversion. When this is not the case, the accuracy of the square-law equations is poor. For negative values of V_{eff}, the transistor is in weak inversion and is said to be operating in the subthreshold region. In this regime, the dominant physical mechanism for conduction between drain and source is diffusion, not drift as in strong inversion, and the transistor is more accurately modelled by an exponential relationship between its control voltage (at the gate) and current, somewhat similar to a bipolar transistor. In the subthreshold region, the drain current is approximately given by an exponential relationship.

$$I_{D(sub)} \cong I_{D0} \frac{W}{L} e^{\left(qV_{eff}/nkT\right)} \qquad 1.17$$

Where $n = \frac{C_{ox}+C_{j0}}{C_{ox}}$ and $I_{D0} = (n-1)\mu_n C_{ox}(\frac{kT}{q})^2$

1.7.2 Mobility Degradation

Transistors, subjected to large electric fields experience degradation in the effective mobility of their carriers. Large lateral electric fields, as shown in Fig. 1.7 for an NMOS device, accelerate carriers in the channel up to a maximum velocity, approximately 107 cm/s in silicon. This is referred to as velocity saturation. Vertical electric fields greater than approximately 5·106 V/m cause the effective channel depth to decrease and also cause more

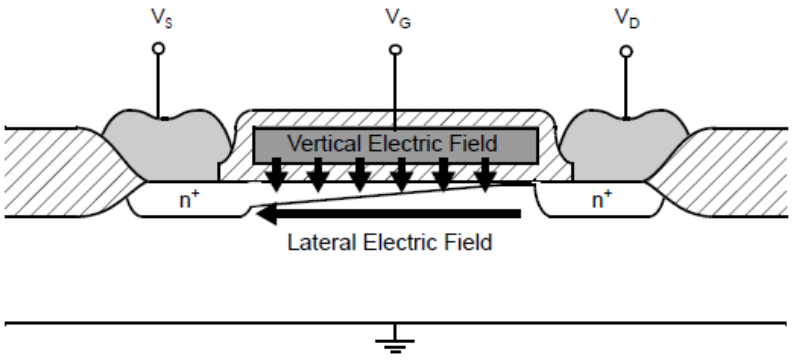


Figure 1.7 NMOS device with lateral and vertical electric field components.[1]

charge carrier collisions. For the purposes of design, these effects may be modelled together by an effective carrier mobility that decreases at high V_{eff},

$$\mu_{n,eff} \cong \frac{\mu_n}{([1+(\theta V_{eff})^m])^{1/m}} \quad 1.18$$

where θ and m are device parameters. Substituting the effective carrier mobility, $\mu_{n\text{-}eff}$, in place of u_n gives a new expression for the drain current incorporating mobility degradation which is

$$I_D \cong \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{eff}{}^2\frac{1}{([1+(\theta V_{eff})^m])^{1/m}} \quad 1.19$$

1.7.3 Short-Channel Effects

A number of short-channel effects degrade the operation of MOS transistors as device dimensions are scaled down. These effects include reduced output impedance and hot-carrier effects (such as oxide trapping and substrate currents). A reduced output impedance is because of depletion region variations at the drain end (which affect the effective channel length) have an increased proportional effect on the drain current. In addition, a phenomenon known as drain-induced barrier lowering (DIBL) effectively lowers V_t as V_{DS} is increased, thereby further lowering the output impedance of a short-channel device.

Another important short-channel effect is due to hot carriers. These high-velocity carriers can cause harmful effects, such as the generation of electron-hole pairs by impact ionization and avalanching. These extra electron-hole pairs can cause currents to flow from the drain to the substrate, as shown in Figure 1.8.

This effect can be modelled by finite drain-to-ground impedance. As a result, this effect is one of the major limitations on achieving very high output impedances of cascode current sources. Another hot-carrier effect occurs when electrons gain energies high enough to tunnel into and possibly through the thin gate oxide. Thus, this effect can cause dc gate currents. However, often more harmful is the fact that any charge trapped in the oxide will cause a shift in transistor threshold voltage. As a result, hot carriers are one of the major factors limiting the long-term reliability of MOS transistors.

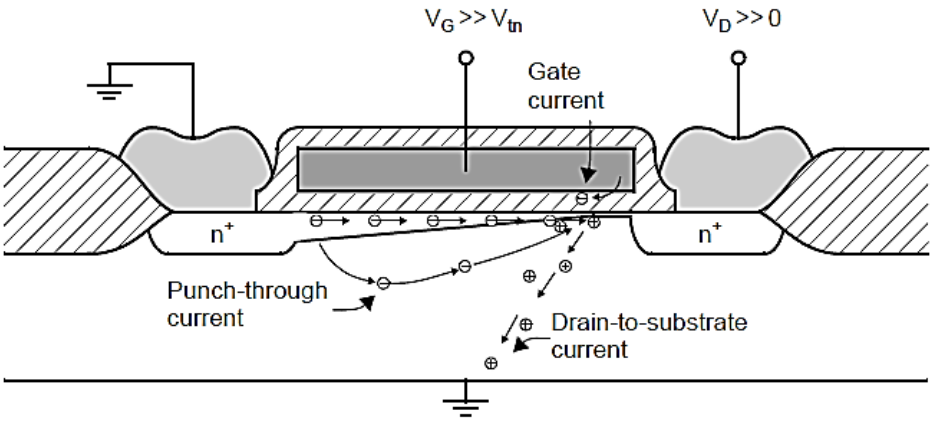


Figure 1.8 Hot carrier effects in an n-channel MOS transistor. [1]

A third hot-carrier effect occurs when electrons with enough energy punch through from the source to the drain. As a result, these high-energy electrons are no longer limited by the drift equations governing normal conduction along the channel. This mechanism is somewhat similar to punch-through in a bipolar transistor, where the collector depletion region extends right through the base region to the emitter. In a MOS transistor, the channel length becomes effectively zero, resulting in unlimited current flow (except for the series source and drain impedances, as well as external circuitry). This effect is an additional cause of lower output impedance and possibly transistor breakdown.

1.7.4 Leakage Currents

Leakage currents impose limitations on how long a dynamically charged signal can be maintained in a high impedance state and on the minimum power consumption achievable when an analog circuit is in an idle (power down) state. Three leakage currents are important in MOS transistors: subthreshold leakage, gate leakage, and junction leakage. Of these, subthreshold leakage is often the largest. It results in a finite drain current even when the transistor is off, Gate leakage results from quantum-mechanical tunnelling of electrons through very thin gate oxides, and can be significant in digital circuits and when large gate areas are used, for example to implement a capacitor. Finally, the reverse-biased source-body and drain-body pn junctions conduct a finite leakage current. The leakage current of a reverse-biased junction (not close to breakdown) is approximately given by

$$I_{lk} = \frac{qA_j n_i}{2\tau_0} X_d \qquad 1.20$$

Where A_j is junction area, n_i is intrinsic concentration of carriers in undoped silicon, τ_0 is effective minority carrier lifetime, X_d is the thickness of the depletion region,

1.8 SPICE Modelling Parameters

Modern MOS models are quite complicated, so only some of the more important MOS parameters used in SPICE simulations are described here. These parameters are used in what are called the Level 2 or Level 3 models. The model level can be chosen by setting the SPICE parameter LEVEL to either 2 or 3. The oxide thickness, t_{ox}, is specified using the SPICE parameter TOX. If it is specified, then it is not necessary to specify the thin gate-oxide capacitance (C_{ox}, specified by parameter COX). The mobility, μ_n, can be specified using UO. The transistor threshold voltage at, V_s=0V, V_{tn} is specified by VTO. The body-effect parameter, γ can be specified using GAMMA. The output impedance constant, λ, can be specified using LAMBDA. Normally, LAMBDA should not be specified since it takes precedence over internal calculations and does not change the output impedance as a function of different transistor lengths or bias voltages. Indeed, modelling the transistor output impedance is one of weakest points in SPICE. If LAMBDA is not specified, it is calculated automatically. The surface inversion potential, $|2\phi_F|$, can be specified using PHI, or it will be calculated automatically. Another parameter usually specified is the lateral diffusion of the junctions under the gate, L_D, which is specified by LD. For accurate simulations, one might also specify the resistances in series with the source and drain by specifying RS and RD.

The capacitances under the junctions per unit area at 0-V bias, (i.e.,C_{j0}) can be specified using CJ or can be calculated automatically from the specified substrate doping.

Table 1.1 0.8μm Cmos technolgy parameters

SPICE Parameter	Model Constant	Brief Description	Typical Value
VTO	V_{tn}:V_{tp}	Transistor threshold voltage (in V)	0.8:–0.9
UO	μ_n:μ_p	Carrier mobility in bulk (in $cm^2/V{\cdot}s$)	500:175
TOX	t_{ox}	Thickness of gate oxide (in m)	1.8×10^{-8}
LD	L_D	Lateral diffusion of junction under gate (in m)	6×10^{-8}
GAMMA	γ	Body-effect parameter	0.5: 0.8
NSUB	N_A:N_D	The substrate doping (in cm^{-3})	3×10^{16}:7.5×10^{16}
PHI	$\lvert 2\phi_F \rvert$	Surface inversion potential (in V)	0.7
PB	Φ_0	Built-in contact potential of junction to bulk (in V)	0.9
CJ	C_{j0}	Junction-depletion capacitance at 0-V bias (in F/m^2)	2.5×10^{-4}:4.0×10^{-4}
CJSW	$C_{j\text{-}sw0}$	Sidewall capacitance at 0-V bias (in F/m)	2.0×10^{-10}:2.8×10^{-10}
MJ	m_j	Bulk-to-junction exponent (grading coefficient)	0.5
MJSW	$m_{j\text{-}sw}$	Sidewall-to-junction exponent (grading coefficient)	0.3

The sidewall capacitances at 0 V, $C_{j\text{-}sw0}$, should normally be specified using CJSW because this parameter is used to calculate significant parasitic capacitances. The bulk grading coefficient specified by MJ can usually be defaulted to 0.5. Similarly, the sidewall grading coefficient specified by MJSW can usually be defaulted to 0.33 (SPICE assumes a graded junction). The built-in bulk-to-junction contact potential, $|\phi_0|$, can be specified using PB or defaulted to 0.8 V. Sometimes the gate-to-source or drain-overlap capacitances can be specified using CGSO or CGDO, but normally these would be left to be calculated automatically using COX and LD. [1] Table 1.1 lists reasonable parameters for a typical 0.8μm CMOS technology.

1.9 Advanced SPICE Models of MOS Transistors

Although the SPICE model parameters presented in the last section provide reasonable accuracy for long-channel devices, for channel lengths L<< 1μm ,their accuracy becomes very poor. Many SPICE MOS models have therefore been developed to try to capture higher-order effects. A summary of the capabilities of the more common modern SPICE model formats is provided in Table 1.2. Unfortunately, these SPICE models require over 100 parameters to accurately capture transistor operation in all of its modes over a wide range of temperatures. Many parameters are required because, for very small device sizes, fundamental constants such as threshold voltage and effective carrier mobility become dependent on the transistor's exact width and length. Hence, it is strongly recommended that analog designers use only a small set of "unit-sized" transistors, forming all transistors from parallel combinations of these elementary devices.

Table 1.2 A summary of modern SPICE model formats.

SPICE Model	Main strengths compared with previous device models
BSIM3	Improved modeling of moderate inversion, and the geometry-dependence of device parameters. This also marked a return to a more physics-based model as opposed to the preceding highly empirical models.
EKV	Relates terminal currents and voltages with unified equations that cover all modes of transistor operation, hence avoiding discontinuities at transitions between, for example, weak and strong inversion. Also handles geometry-dependent device parameters.
BSIM4	Improved modeling of leakage currents and short-channel effects, noise, and parasitic resistance in the MOSFET terminals, as well as continued improvements in capturing the geometry-dependence of device parameters.
PSP	Improved modeling of noise and the many short-channel and layout-dependent effects now dominant in nanoscale CMOS devices. Particular effort was made to accurately model nonlinearities, which requires accuracy in the high-order derivatives of the transistor's voltage–current relationships.

1.10 Passive Devices

Passive components are often required for analog design. However, since transistor performance is the primary consideration in the development of most integrated-circuit fabrication technologies, integrated-circuit passive components exhibit significant non-idealities that must be understood by the analog designer. The most common passive components in analog integrated-circuit design are resistors and capacitors.

1.10.1 Resistors

Sheet Resistor: The simplest realization of an integrated-circuit resistor is nothing more than a strip of conductive material above the silicon substrate. The conductivity of the material from which the strip is made is generally characterized by its sheet resistance, R_S, This, along with the dimensions of the strip, determines the value of the resistor.[1]

$$R = R_S \frac{W}{L} \qquad 1.21$$

1.10.2 Semiconductor Resistors

Integrated-circuit manufacturing processes that are developed primarily for digital design may not include any materials with sufficient sheet resistance to realize practically useful resistor values. In these processes, a lightly doped section of the silicon substrate with contacts at either end may be used as a resistor. type-n resistor in a p-substrate is shown in Figure 1.9. The resistor is isolated from the grounded substrate by a reverse-biased pn-junction. Depending on the dopant concentration, the effective sheet resistance may be in the range of 10's of Ohms with complex temperature dependence.

The resistance of above resistor is found by

$$R = \frac{W}{q\mu_n H n_n} \qquad 1.22$$

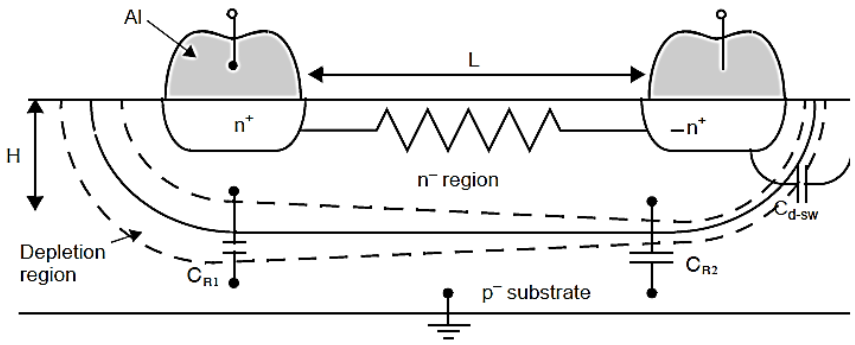


Figure 1.9 A resistor made from a lightly doped semiconductor region with depletion region capacitances [1]

Where H is height of device, n_n is the doping concentration.

1.10.3 Capacitors

PN Junction Capacitors

The capacitance can be realised by reverse biased pn-junctions. Junction capacitances may be introduced intentionally into an analog design to serve as a capacitor. They provide a relatively high value of capacitance per unit area since the depletion region can be quite thin and the relative permittivity of silicon is quite high (K_S= 11.8). Their capacitance can be tuned by adjusting the voltage across them. Unfortunately, several features of junction capacitances pose problems for analog design. First, although the tunability of their capacitance is useful in some applications, it also makes them nonlinear elements that distort time-varying signals. Second, the value of capacitance realized by a given size junction varies considerably with dopant concentration which is difficult to control during integrated circuit manufacturing. Finally, junction capacitors have more leakage current than other types of integrated circuit capacitors. The most common application for pn junction capacitors is as a varactor in tunable radio-frequency circuits, notably oscillators, although even there MOS capacitors are now often favoured.

MOS Capacitors

Since the gate oxide is the thinnest dielectric available in an integrated circuit, it is imminently sensible to build capacitors around it. There are many ways to do so. All comprise gate and silicon conducting “plates” separated by the gate oxide as a dielectric. All are nonlinear capacitors, whose value depends on the voltage across it. When using a PMOS transistor, one terminal is the gate and the other is the source, drain, and body all shorted together underneath. In this configuration, V_{DS}=0 and V_{SG} = - V_{GS} is the voltage on the capacitor.

If $V_{GS} > |V_{tp}|$ the device enters triode and the small-signal capacitance is given by

$$C_{MOS(on)} = WLC_{ox} + 2WL_{ov}C_{ox} \quad (1.23)$$

$$C_{MOS(off)} = 2WL_{ov}C_{ox} \quad (1.24)$$

Clearly this is a highly nonlinear capacitor and should be used with care in analog design. Nevertheless, it is popular for three reasons. First, it is relatively well-modelled by standard circuit simulators. Second, the very thin gate oxide ensures a high capacitance-per-unit-area. Third, it requires no special modifications to CMOS integrated-circuit fabrication processes.

Metal-metal

To realize a purely linear capacitance on an integrated circuit, it is necessary to avoid the use of semiconductors for either plate. Instead, the many electrically-isolated layers of conductors above the silicon substrate are used. Two different geometries used to implement metal-metal capacitors are shown in Figure 1.10. The capacitance of the parallel-plate structure is approximately

$$C = \frac{\varepsilon_{ox} A}{t_{ox}} \qquad 1.25$$

t_{ox} is the spacing between plates

ε_{ox} is the permittivity of the insulator between plates

A is area of the plate

The parallel-plate structure is asymmetric since the bottom plate is in closer proximity to the silicon substrate and electrically shields the top plate from ground. Hence, the bottom plate has a larger parasitic capacitance. This can often be exploited in analog designs by connecting the bottom plate to a node with a constant potential with respect to ground, thus minimizing parasitics on the plate with time-varying potential.

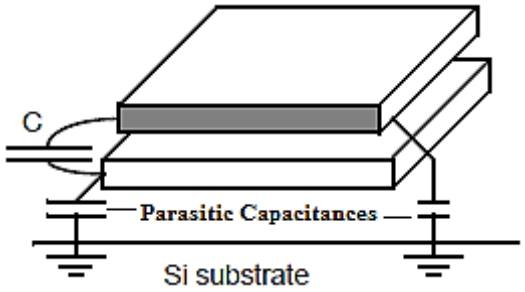


Figure1.10 Metal-metal parallel plate capacitor

2. Basic Current Mirror and Single Stage Amplifiers

2.1 Simple Current Mirror Circuit

An ideal current mirror is a two-port circuit that accepts an input current I_{in} and produces an output current $I_{out}=I_{in}$. An ideal current source has a high output resistance and, hence, so will an ideal current mirror. In this way, the ideal current mirror faithfully reproduces the input current regardless of the source and load impedances to which it is connected. A simple CMOS current mirror is shown in Figure 2.1, in which it is assumed that both transistors are in the active region, which means that the drain voltage of Q_2 must be greater than V_{eff2}. If the finite small-signal drain-source impedances of the transistors are ignored, and it is assumed that both transistors are the same size, then and will have the same current since they both have the same gate-source voltage. However, when finite drain-source impedance is considered, whichever transistor has a larger drain-source voltage will also have a larger current.

2.2 Common Source Amplifier

A simple current mirror can be used as an active load in a common source amplifier as shown in Figure 2.2. This common-source topology is the most popular gain stage, especially when high input impedance is desired. In the figure 2.2 a n-channel common-source amplifier has a p-channel current mirror used as an active load to supply the bias current for the drive transistor. By using an active load, a high-impedance output load can be realized without using excessively large resistors or a large power-supply voltage. As a result, for a given power supply voltage, a larger voltage gain can be achieved using an active load than would be possible if a resistor were used for the load. For example, if a 100-kΩ load were required with a 100μA bias current, a resistive-load approach would require a power-supply voltage of 100 kΩ X 100μA=10V. An active load takes advantage of the nonlinear, large-signal transistor current–voltage relationship to provide large small-signal resistances without large dc voltage drops.[1]

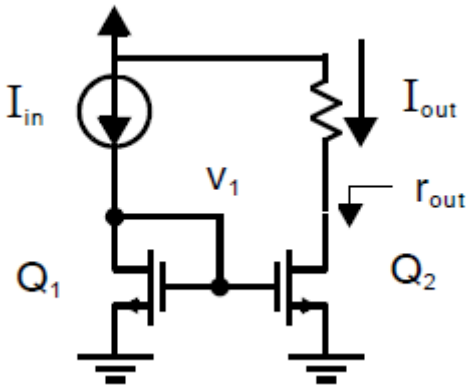


Figure 2.1 Current Mirror Circuit

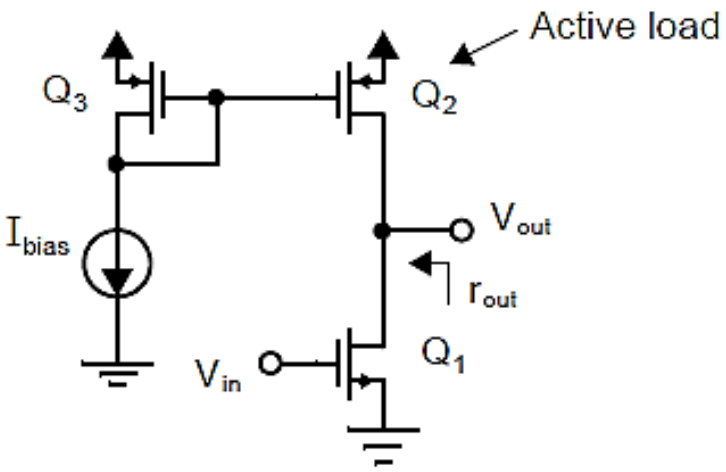


Figure 2.2 Common Source Amplifier

Voltage gain of single stage common source amplifier is given by

$$A_v = -(g_{m1}r_{01})\frac{r_{02}}{r_{02}+r_{01}} = -g_{m1}(r_{o1}||r_{o2}) \qquad 2.1$$

Where g_{m1} is transconductance of Q_1, r_{o1} and r_{o2} are output resistance of Q_1 and Q_2

2.3 Common Drain amplifier

Another general use of current mirrors is to supply the bias current of source-follower amplifiers, as shown in Figure 2.3. In this example, Q_1 is the source follower and Q_2 is an active load that supplies the bias current of Q_1. These amplifiers are commonly used as *voltage buffers* and are therefore commonly called source followers. They are also referred to as common-drain amplifiers, since the input and output nodes are at the gate and source nodes, respectively, with the drain node being at small-signal ground. Although the dc level of the output voltage is not the same as the dc level of the input voltage, ideally the small-signal voltage gain is close to unity. In reality, it is somewhat less than unity. However, although this circuit does not generate voltage gain, it does have the ability to generate current gain.

The voltage gain of Common drain amplifier is given by

$$A_v = \frac{g_{m1}}{g_{m1}+g_{ds1}+g_{ds2}} \qquad 2.2$$

Where g_{ds1} and g_{ds2} are drain- source conductances.

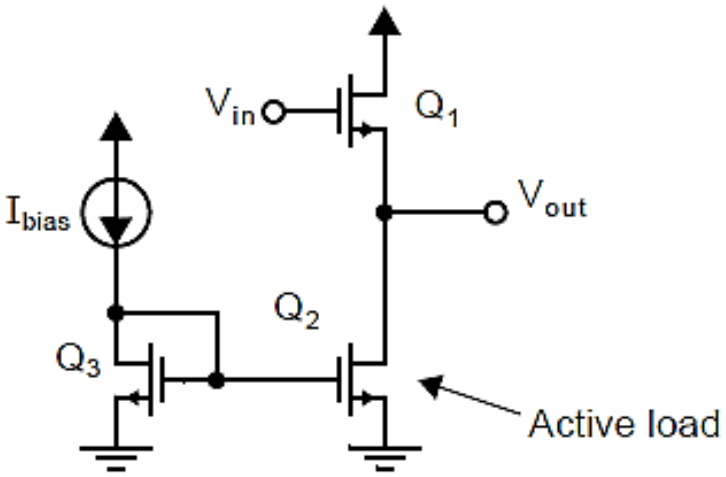


Figure 2.3 Common Drain Amplifier

2.4 Common Gate Amplifier

A common-gate amplifier with an active load is shown in Figure 2.4. This stage is commonly used as a gain stage when relatively small input impedance is desired. For example, it might be designed to have an input impedance of 50Ω to terminate a 50Ω transmission line. Another common application for a common-gate amplifier is as the first stage of an amplifier where the input signal is a current; in such cases a small input impedance is desired in order to ensure all of the current signal is drawn into the amplifier, and none is "lost" in the signal source impedance. Aside from its low input impedance, the common gate amplifier is similar to a common-source amplifier; in both cases the input is applied across V_{gs}, except with opposite polarities, and the output is taken at the drain. Hence, in both cases the small signal gain magnitude approximately equals the product of g_m and the total impedance at the drain.

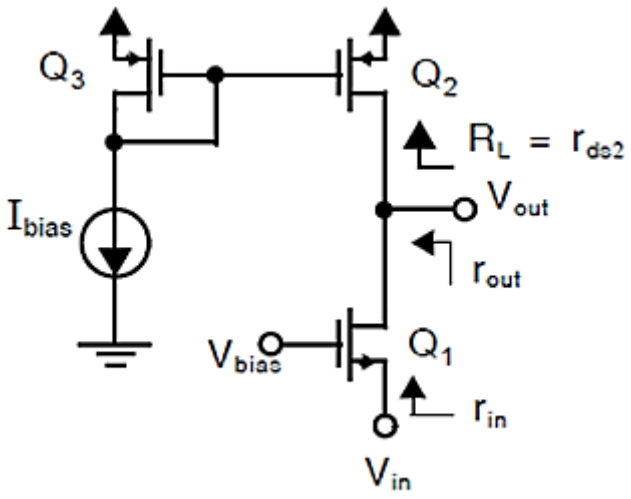


Figure 2.4 Common Gate Amplifier

The voltage gain of Common gate amplifier is given by

$$A_v = \frac{g_{m1}(R_L||r_{ds1})}{1+R_s(\frac{g_{m1}+g_{ds1}}{1+{}^{R_L}/_{r_{ds1}}})} \quad 2.3$$

The input impedance of above amplifier is

$$r_{in} = \frac{1}{g_{m1}}(1+\frac{R_L}{r_{ds1}}) \quad 2.4$$

2.5 Cascode Current Mirror

A cascode current mirror is shown in Figure 2.5. The output impedance looking into the drain of Q_2 is simply r_{ds2}, which is seen using small signal analysis. Thus, the output impedance can be immediately derived by considering Q_4 as a current source with a source-degeneration resistor of value r_{ds2}.

So $r_{out} = r_{ds4}[1 + R_s(g_{m4} + g_{s4} + g_{ds4})]$

$r_{out} = r_{ds4}[1 + r_{ds2}(g_{m4} + g_{s4} + g_{ds4})]$

$$= r_{ds4}r_{ds2}g_{m4} \quad 2.5$$

Thus, the output impedance has been increased by a factor of $g_m r_{ds4}$ which is an upper limit on the gain of a single-transistor MOS gain-stage and might be a value between 10 and 100, depending on the transistor sizes and currents and the technology being used.

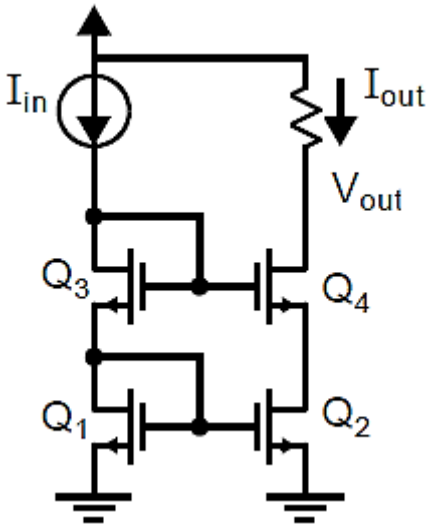


Figure 2.5 Cascode Current Mirror

This significant increase in output impedance can be instrumental in realizing single stage amplifiers with large low-frequency gains. The disadvantage in using a cascode current mirror is that it reduces the maximum output voltage swings possible before transistors enter the triode region.

2.6 Cascode Gain Stage

In modern IC design, a commonly used configuration for a single-stage amplifier is a cascode configuration. This configuration consists of a common source connected transistor feeding into a common-gate-connected transistor. Two examples of cascode amplifiers are shown in Figure 2.6. The configuration in Figure 2.6(a) has both an n-channel common-source transistor, Q_1 and an n-channel common-gate cascode transistor, Q_2. This configuration is sometimes called a telescopic-cascode amplifier. The configuration shown in Figure 2.6(b) has an n-channel input (or drive) transistor, but a p-channel transistor is used for the cascode (or common-gate) transistor. This configuration is usually called a folded-cascode stage. When incorporated into an operational amplifier, the folded cascode can provide greater output swing than the telescopic cascode. However, the folded cascode usually consumes more power since the drain bias currents for Q_1 and Q_2 are drawn in parallel from the supply voltage, whereas in the telescopic cascode, the same dc drain current is shared by both transistors. There are two major reasons for the popularity of cascode stages. The first is that they can have quite large gain for a single stage due to the large impedances at the output. To enable this high gain, the current sources connected to the output nodes are realized using high quality cascode current mirrors. The second major reason for the use of cascode stages is that they limit the voltage across the input drive transistor. This minimizes any short channel effects, which becomes more important with modern technologies having very short channel-length transistors. It can also permit the circuit to handle higher output voltages without risking damage to the common-source transistor [1].

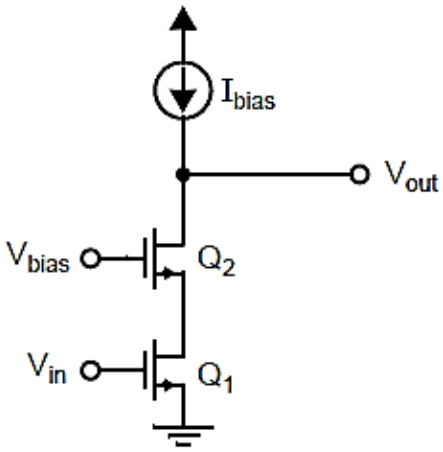
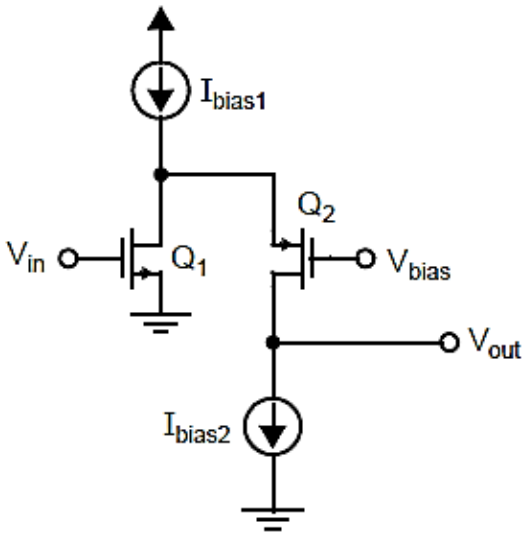


Figure 2.6(a) Telescopic Cascode Amplifier



2.6(b) Folded Cascode Amplifier

The main drawback of cascode amplifiers is that the output voltage is restricted to a narrower range than the common-source amplifier in order to keep all devices in the active region. This is because some voltage must be kept between drain and source of the extra cascode transistor, Q_2.

From the section on cascode current-mirrors, we know that the impedance looking into the drain of cascode is

$$r_{d2} = g_{m2} r_{ds1} r_{ds2} \qquad 2.6$$

$$R_{out} = r_{d2} || R_L$$

where R_L is the output impedance of bias current source.

The trans-conductance looking into the source of common gate transistor Q_2

$$g_{in2} = {}^{1}/_{r_{in2}} \cong \frac{g_{m2}}{1+\frac{R_L}{r_{ds2}}} \qquad 2.7$$

The Gain from input to source of Q_2 is simply that of a common-source amplifier with a load resistance of r_{in2} and is therefore given by

$$\frac{V_{s2}}{V_{in}} = -g_{m1}(r_{ds1} || r_{in2}) = -\frac{g_{m1}}{g_{ds1}+g_{in2}} \qquad 2.8$$

The gain from the source of Q_2 to the output is simply that derived earlier for the common-gate stage.

$$\frac{V_{out}}{V_{s2}} = \frac{g_{m2}+g_{s2}+g_{ds2}}{g_{ds2}+G_L} \cong \frac{g_{m2}}{g_{ds2}+G_L} \qquad 2.9$$

Overall voltage gain $A_V = \frac{V_{s2}}{V_{in}} \frac{V_{out}}{V_{s2}} \cong -g_{m1} g_{m2} (r_{ds1} || r_{in2})(r_{ds2} || R_L)$ 2.10

3. Implementation of Two Stage Common Source Amplifier

In this chapter, a Common Source amplifier is investigated using LT SPICE simulation tool. A CMOS common source amplifier as shown in figure 3.1 is designed and implemented using LT SPICE tool. CMOS technology-5µm is considered for the MOSFETs shown in the circuit diagram. To specify the dimensions of the MOSFETs in LT Spice, the multiplicative factor 'm' together with the channel length 'L' and the channel width 'W' are used. The MOSFET parameter 'm', whose default value is 1, is used in SPICE to specify the number of MOSFETs connected in parallel [2].

The drain current of A MOSFET is given by

$$I_D = \tfrac{1}{2}\mu C_{ox} m V_{eff} \frac{W}{L} \qquad 3.1$$

The CS amplifier in Figure 3.1 is designed for a bias current of 100µA assuming a reference current I_{ref} = 100µA and V_{DD} = 10V. Transistors M_2 and M_3 form a current mirror pair which is an active load for common source configured MOSFET M_1.

To compute the dc transfer characteristic of the CS amplifier, we perform a dc analysis in LT Spice with V_{in} swept over the range 0 to V_{DD} and plot the corresponding output voltage V_{out}. Figure 3.2 shows the resulting transfer characteristic. The slope of this characteristic (i.e.,dV_{out}/dV_{in}) corresponds to the gain of the amplifier. The high-gain segment is clearly visible for V_{in} around 1.5V. This corresponds to an effective voltage for M_1 of Veff = V_{in}-V_{tn} = 0.5V, as desired. From the dc transfer characteristic that for an input dc bias of V_{in} = 1.5V, the output dc bias is V_{out} = 4.88 V. This choice of V_{in} maximizes the available signal swing at the output by setting V_{out} at the middle of the linear segment of the dc transfer characteristic [3].

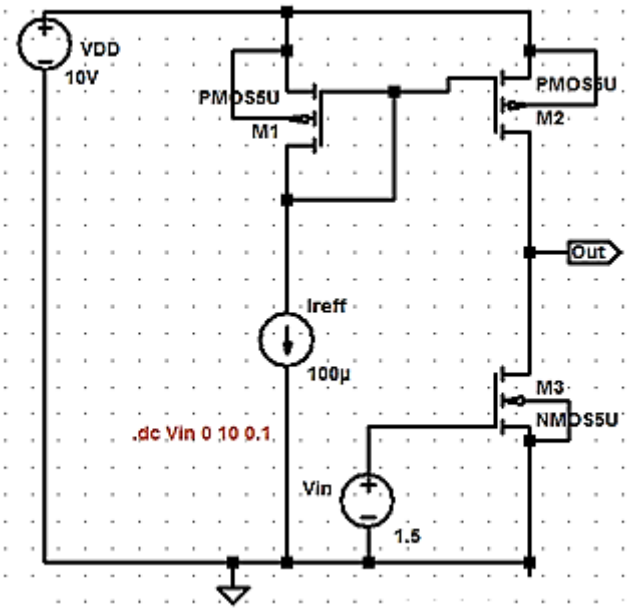


Figure 3.1 Common Source Configuration

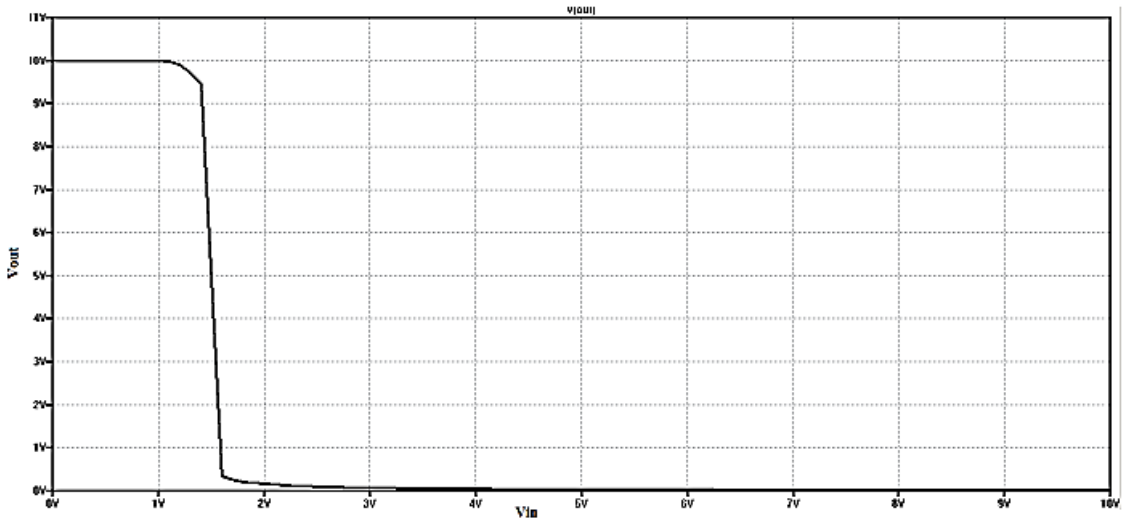


Figure 3.2 Transfer Characteristics of Common source Configuration

The CS amplifier in Figure 3.3 is designed assuming a reference current I_{ref} =100 μA and V_{DD}= 3.3V. The current-mirror transistors, M_2 and M_3, are sized for V_{OV2} = V_{OV3} = 0.5V, while the input transistor M_1 is sized for V_{0Vl}=0.15V. Unit-size transistors are used with W/L = 1.25μm/0.6 μm for the NMOS devices and W/L = 5 μm /0.6 μm for the PMOS devices. Thus, using 0.5- μm CMOS process parameters we find m_1=18 and m_2= m_3 = 4.

$$G_v = -g_{m1}R_{L'} = -g_{m1}(r_{o1}||r_{o2}) = -\frac{2}{V_{OV1}}\left(\frac{V_{An}V_{Ap}}{V_{An}+V_{Ap}}\right) \cong -44.4V/V \qquad 3.2$$

The dc bias voltage of the signal source is set such that the voltage at the source terminal of M_1 is V_{S1}=1.3V. This requires the dc level of V_{sig} to be V_{OV1} + V_{tn1} + V_{S1} = 2.45 V because V_{tnl}=1V as a result of the body effect on M_1.

A bias-point simulation is performed in LT-Spice to verify that all MOSFETs are biased in the saturation region. Next, to compute the frequency response of the amplifier, we set the ac voltage of the signal source to 1V, perform an AC-analysis simulation, and plot the output voltage magnitude versus frequency. Figure 3.4 shows the resulting frequency response for R_{sig} = 1MΩ. A load capacitance of C_{load} = 0.5 pF is used. The corresponding value of the 3-dB frequency f_H of the amplifier is 256.2kHz.

Theoretically, $$f_H = \frac{1}{2\pi R_{sig}C_{in}} \qquad 3.3$$

$$C_{in} = C_{gs1} + C_{gd1}(1 + g_{m1}R'_L) \qquad 3.4$$

$$= \left(\frac{2}{3}m_1W_1L_1C_{ox} + C_{gs,ov1}\right) + C_{gd,ov1}(1 + g_{m1}R'_L) \qquad 3.5$$

$$R'_L = r_{o1}||r_{o2} \qquad 3.6$$

Where $r_o = \frac{1}{\lambda I_D}$ 3.7

$C_{gs,ov1}$ and $C_{gd,ov1}$ are found from process parameters as shown below

$$C_{gs,ov1} = m_1 W_1 CGSO \quad 3.8$$

$$C_{gd,ov1} = m_1 W_1 CGDO \quad 3.9$$

This results in C_{in} = 0.53pF when $|G_v| = g_{m1}R_L'$=53.2V/V. accordingly f_H will be 300.3kHz, which is closed to the value computed by LTspice

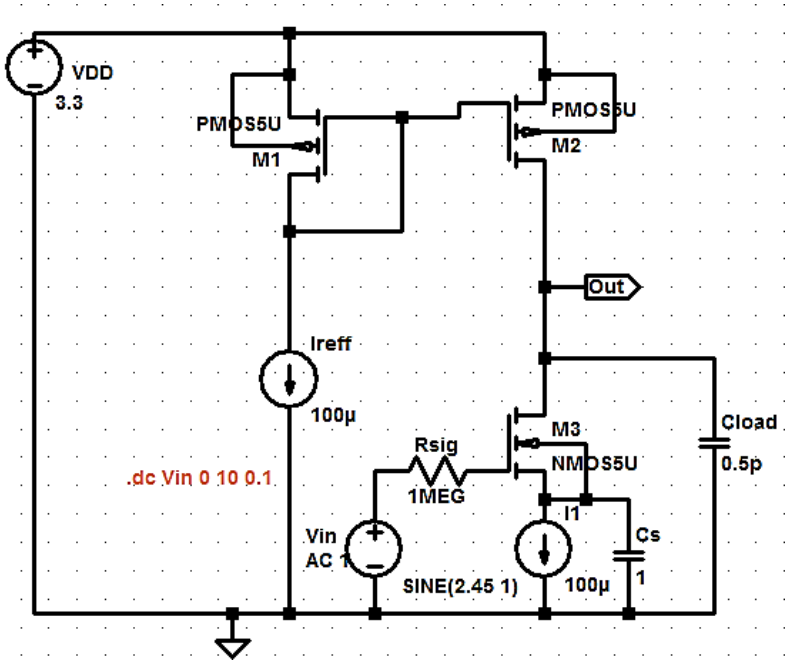


Figure 3.3 Common Source Amplifier

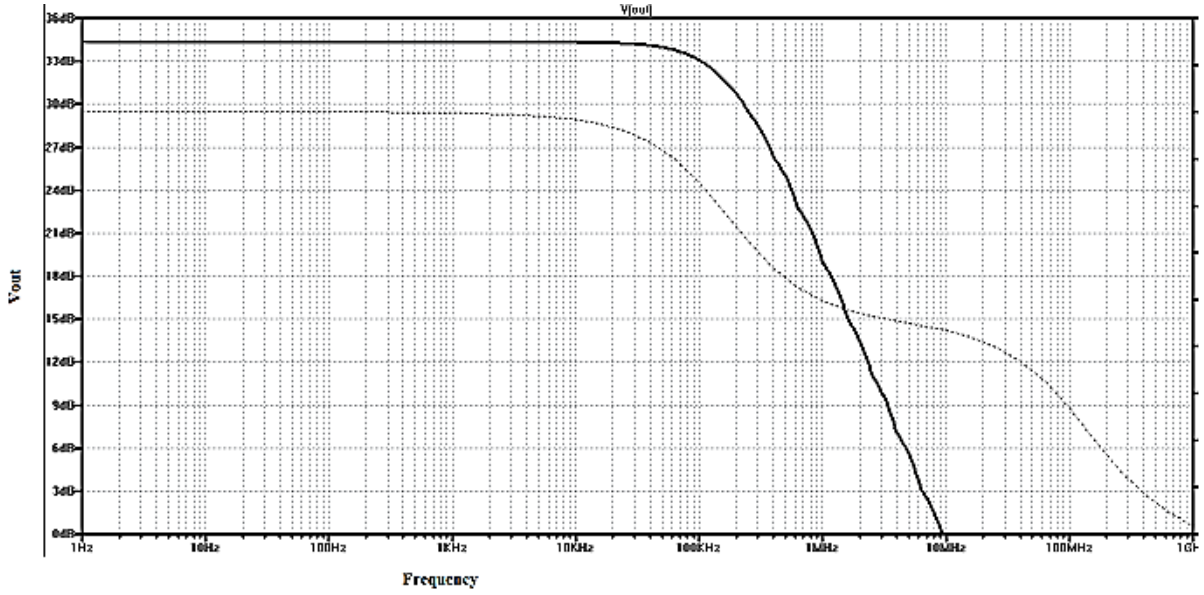


Figure 3.4 Frequency Response of Common Source Amplifier

4. Implementation of CMOS Cascode Amplifier

By placing a common-gate amplifier stage in cascade with a common source amplifier stage, a very useful and versatile amplifier circuit results. It is known as the cascode configuration and has been in use for nearly three quarters of a century, obviously in a wide variety of technologies. The basic idea behind the cascode amplifier is to combine the high input resistance and large transconductance achieved in a common source amplifier with the current buffering property and the superior high-frequency response of the common-gate circuit. The cascode amplifier can be designed to obtain a wider bandwidth but equal dc gain as compared to the common source amplifier. Alternatively, it can be designed to increase the dc gain while leaving the gain bandwidth product unchanged.

To avoid the problem of stacking a large number of transistors across a low-voltage power supply, one can use a PMOS transistor for the cascode device, as shown in Figure 4.1. A NMOS transistor M_1 is operating in the Common Source configuration and Common Gate stage is implemented using the PMOS transistor M_2. The PMOS current mirror M_3-M_4 and the NMOS current mirror M_5-M_6 are used to realize, respectively, current sources I_1 and I_2 in the circuit. Furthermore, the current transfer ratio of mirror M_3-M_4 is set to 2, this results in I_{D3}= 2*I_{ref}. Hence M_2 is biased at I_{D2}=I_{D3}-I_{D1}=I_{ref}. The gate bias voltage of M_2 is generated using the diode connected transistors M_7 and M_8 [3].

The folded-cascode amplifier in Figure 4.1 is designed assuming a reference current I_{ref} =100μA and V_{DD} = 3.3 V. All transistors are sized for an overdrive voltage of 0.3V, except for the input transistor M_1 which is sized for V_{0Vl} = 0.15V.

Midband Voltage gain of Cascode amplifier is given by

$$G_v = -g_{m1}R_{out} \quad (4.1)$$

Where $R_{out} = R_{out2}||R_{out5}$ (4.2)

R_{out2} is the resistance seen looking into the drain of the cascode transistor M_2, while R_{out5} is the resistance seen looking into the drain of the current mirror transistor M5.

$$R_{out2} \cong (g_{m2}r_{o2})R_{s2} \quad (4.3)$$

Where $R_{s2} = r_{01}||r_{03}$ is the effective resistance at the source of M_2.

$$R_{out5} = r_{o5} \quad (4.4)$$

Thus output resistance of cascode amplifier is

$$R_{out} \cong r_{o5} \quad (4.5)$$

$$G_v \cong -g_{m1}r_{o5} = -2\frac{V_{An}}{V_{OV1}} \quad (4.6)$$

Using the 0.5µACMOS parameters, this gives R_{out}=100kHz and G_v =-133V/V. Figure 4.2 shows the frequency response of the folded-cascode amplifier as computed by LT. The corresponding values of the 3-dB frequency f_H of the amplifier is 1.2MHz.

Theoretically, $f_H = \frac{1}{2\pi R_{sig} C_{in}}$ 4.7

C_{in} of the folded cascode amplifier can be estimated by replacing R_L' in Equation 3.5 with the total resistance R_{dl} between the drain of M1 and ground.

$R_{d1} = r_{01} || r_{03} || R_{in2}$ 4.8

Where Rin2 is the input resistance of common gate transistor M_2 and can be obtained from

$R_{in2} = \frac{r_{02}+r_{05}}{g_{m2} r_{02}}$ 4.9

Thus $R_{d1} \cong r_{o1} || r_{o3} || \frac{r_{o2}+r_{o5}}{g_{m2} r_{o2}} \cong \frac{2}{g_{m2}}$ 4.10

Using 0.5µm CMOS parameters c_{in}=0.1137pF and f_H = 1.4MHz. which approximately matches with SPICE calculated value.

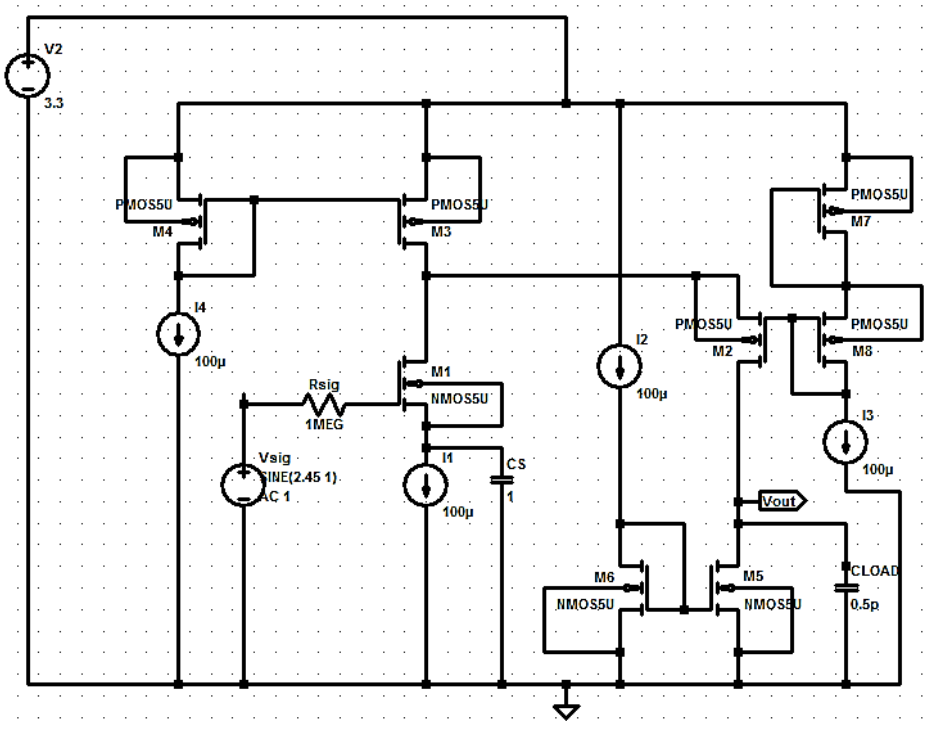


Figure 4.1 Folded Cascode Amplifier

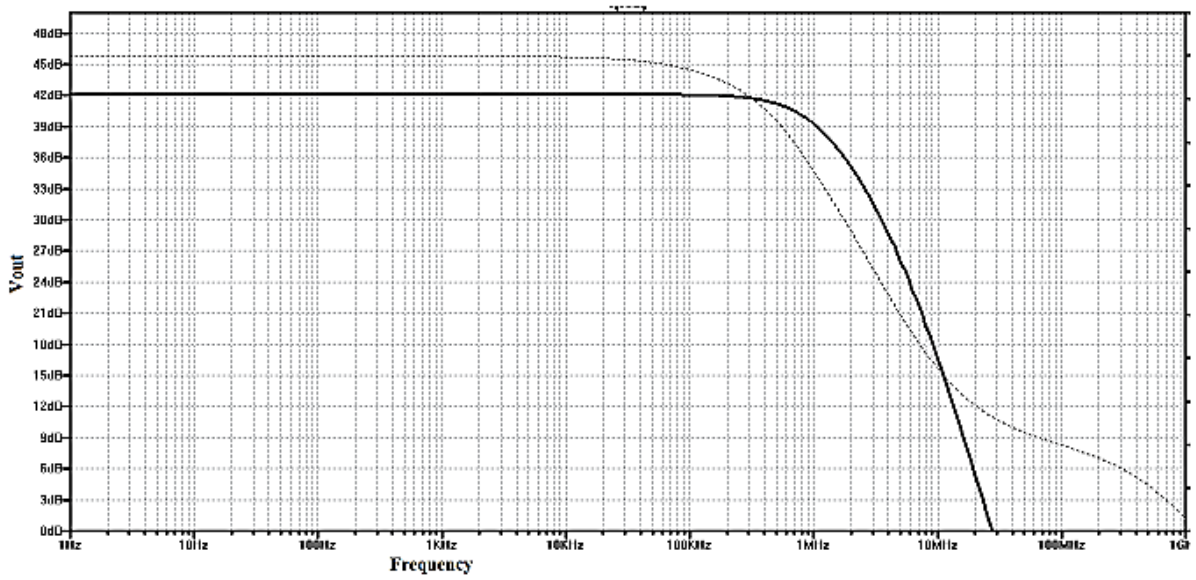


Figure 4.2 Frequency Response of Folded Cascode amplifier

5. Implementation of CMOS Differential Amplifier

In a differential amplifier the output signal is the amplified version of the difference of two inputs of the amplifier. Because of the exclusive properties of this type of amplifier, it is considered as one of the most important building blocks in many analog circuits. Figure 5.1 shows a CMOS differential pair with current mirror active load. This amplifier is regarded as an integral part at the input of most single-ended output operational amplifiers so that many properties of an op amp depend on the parameters of this block. Hence its transient behaviour and frequency response is studied in detail with help of simulation tool.

In Figure 5.1 transistors M_3 and M_4 form a current mirror active load [4-5]. An active load acts as a current source. Thus it must be biased such that their currents add up exactly to I_{bias}. In practice this is quite difficult. Thus a feedback circuit is required to ensure this equality. This is achieved by using a current mirror circuit as load. One transistor (M_3) is always connected as diode and drives the other transistor (M_4). Since $V_{GS3}=V_{GS4}$, if both transistors have the same parameters, then the current I_{D3} is mirrored to I_{D4}, i.e., $I_{D3}=I_{D4}$. The advantage of this configuration is that the differential output signal is converted to a single ended output signal with no extra components required. In this circuit, the output voltage or current is taken from the drains of M_2 and M_4. The operation of this circuit is as follows

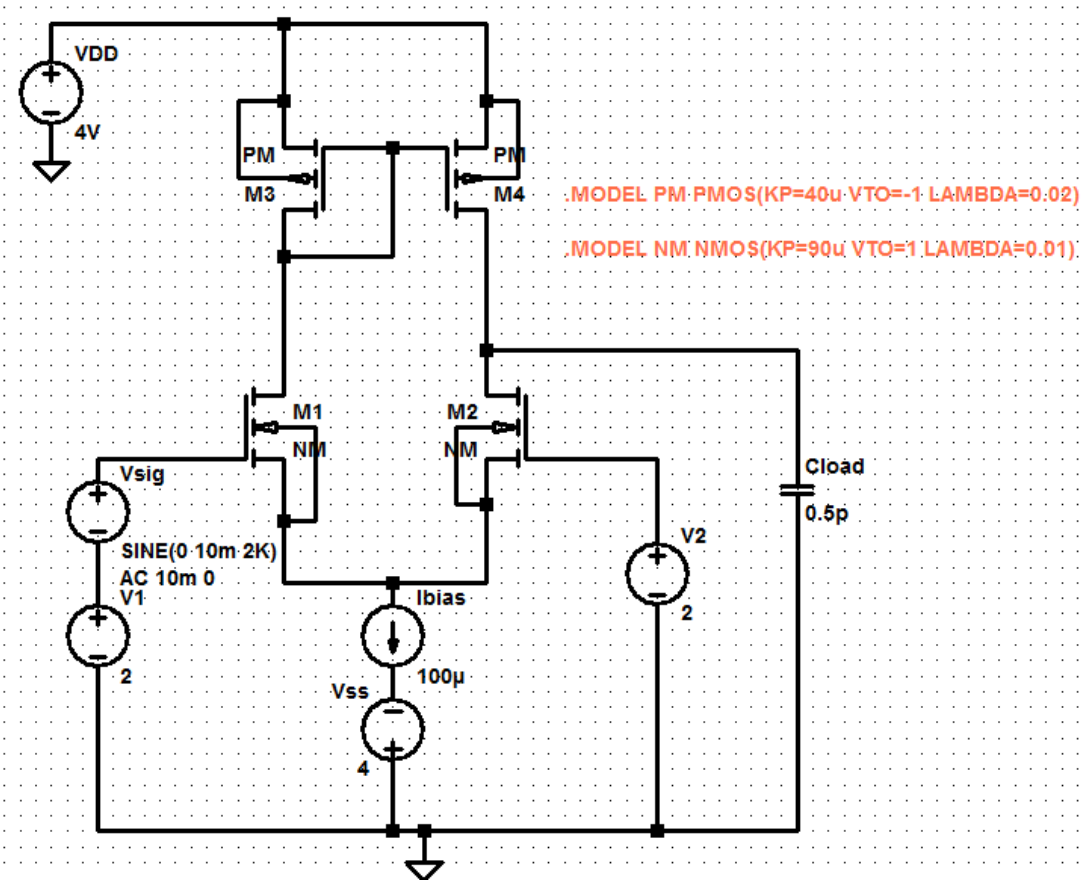


Figure 5.1 CMOS differential pair with current mirror active load

5.1. Small Signal Analysis

The small signal analysis of differential amplifier can be accomplished with the assistance of the model shown in Figure 5.2, which is only appropriate for differential analysis when both sides of the amplifier are assumed to be perfectly matched. If this condition is satisfied, then the point where the sources of M_1 and M_2 are connected can be considered at AC ground. The body effect is neglected.

Output Resistance

The evaluation of the output resistance, r_{out}, is determined by using the small-signal equivalent circuit and applying a voltage to the output node, as seen in Figure 5.2. It must be noted that the T model was used for both M_1 and M_2, whereas M_3 was replaced by an equivalent resistance (since it is diode-connected), and the hybrid-π model was used for M_4.

As usual, r_{out} is defined as the ratio V_x/i_x, where i_x is given by the sum

$$i_x = i_{x1} + i_{x2} + i_{x3} + i_{x4} \quad 5.1$$

$$i_{x1} = \frac{V_x}{r_{ds4}} \quad 5.2$$

$$i_{x2} \cong \frac{V_x}{r_{ds2}+(r_{s1}||r_{s2})} \cong \frac{V_x}{r_{ds2}} \quad 5.3$$

This i_{x2} current splits equally between $i_{s1}$and i_{s2} (assuming r_{s1}= r_{s2} and once again ignoring r_{ds1}), resulting in

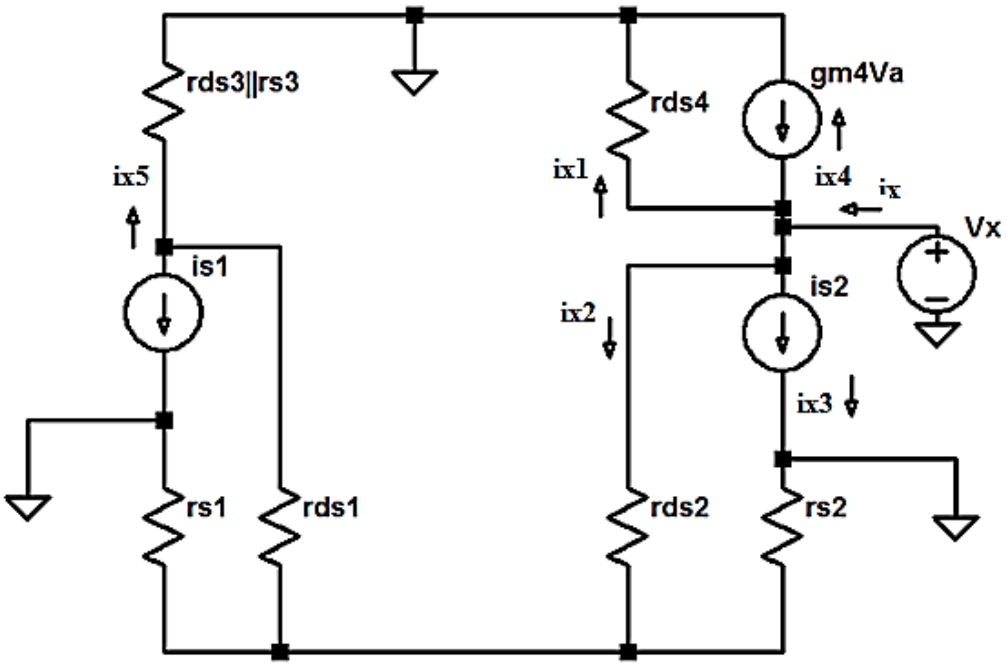


Figure 5.2 Small-signal model for the calculation of output resistance

$$i_{s1} = i_{s2} = \frac{-V_x}{2r_{ds2}} \quad 5.4$$

However, since the current mirror realized by M_3 and M4 results in $i_{x4} = i_{x5}$ (assuming $g_{m4} = 1/r_{s4} = 1/r_{s3}$ and r_{ds3} is much larger than r_{s3}), the current i_{x4} is given by

$$i_{x4} = -i_{s1} = -i_{s2} = -i_{x3} \quad 5.5$$

In other words, when the current splits equally between r_{s1} and r_{s2}, the current mirror of M_3 and M_4 causes the two currents i_{x3} and i_{x4} to cancel each other. Finally, the output resistance, rout, is given by

$$r_{out} = \frac{V_x}{i_{x1}+i_{x2}+i_{x3}+i_{x4}} \quad 5.6$$

$$= \frac{V_x}{V_x/r_{ds4} + V_x/r_{ds2}} \quad 5.7$$

$$r_{out} = (r_{ds2}||r_{ds4}) \quad 5.8$$

5.2 Low frequency voltage gain (Av)

Figure 5.3 shows Small signal model of differential pair with current mirror load. Since, v_{gs3}=$vgs4$. The voltage v_{gs4} can be calculated from above small signal model as

$$v_{gs4} = -g_{m1}\frac{v_{id}}{2}\left(\frac{1}{g_{m3}}||r_{ds1}||r_{ds3}\right) \quad 5.9$$

$$\cong -\frac{g_{m1}}{g_{m3}}\frac{v_{id}}{2} \quad 5.10$$

This voltage controls the drain current of M_4 resulting in a current of $g_{m4}v_{gs4}$. Thus the output current i_{out} will be

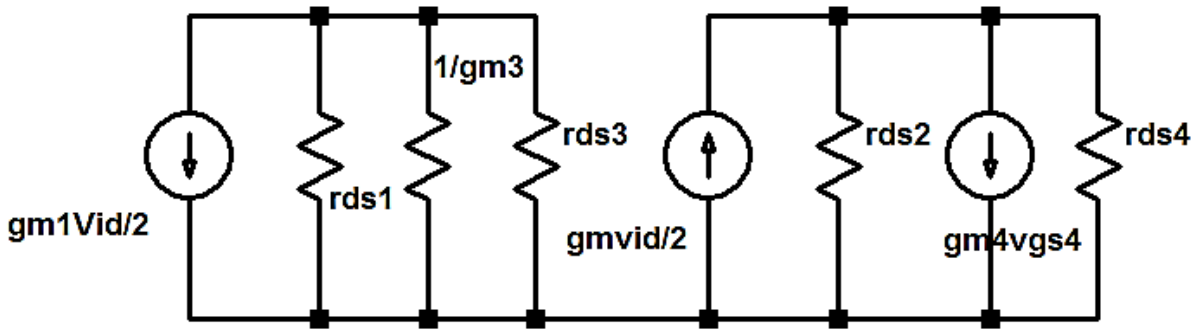


Figure 5.3 Small signal model of differential pair with current mirror load

$$i_{out} = -g_{m4} v_{gs4} + g_{m2} \frac{v_{id}}{2} \quad 5.11$$

$$i_{out} = -g_{m4} \frac{g_{m1}}{g_{m3}} \frac{v_{id}}{2} + g_{m2} \frac{v_{id}}{2} \quad 5.12$$

Since $g_{m3}=g_{m4}$ and $g_{m1}=g_{m2}=g_m$

$$i_{out} = g_m v_{id} \quad 5.13$$

Now small signal output voltage is simply

$$v_{out} = i_{out} r_{out} \quad 5.14$$

$$= g_m v_{id} (r_{ds2} || r_{ds4}) \quad 5.15$$

So voltage gain is

$$A_v = \frac{v_{out}}{v_{id}} = g_m (r_{ds2} || r_{ds4}) \quad 5.16$$

5.3 DC Analysis-Large signal model

The differential pair in Figure 5.3 is biased with a current source so that

$$I_{bias}=I_{d1}+I_{d2} \quad 5.17$$

If we label the input voltages at the gates of M_l and M_2 as $V_{i1}$and V_{i2}, we can write the input difference as

$$V_{di}=V_{i1}-V_{i2}=V_{gs1}-V_{gs2} \quad 5.18$$

or in terms of the AC and DC components of the differential input voltage, V_{di},

$$V_{di}=V_{GS1}+v_{gs1}-V_{GS2}-v_{gs2} \quad 5.19$$

When the gate potentials of M_l and M_2 are equal, then (assuming both are operating in the saturation region)

$$I_{D1}=I_{D2}=I_{bias2}$$

5.4. Maximum and Minimum Differential Input Voltage

Since we know that a saturated MOSFET follows the relation

$$I_d = \frac{\beta_n}{2} (V_{gs} - V_{thn}) \quad 5.20$$

The maximum difference in the input voltages, V (maximum differential input voltage), is found by setting I_{d1} to I(Ml conducting all of the tail bias current) and $I_{d2}$to 0 (M2 off)

$$V_{dimax} < V_{i1} - V_{i2} = \sqrt{\frac{2.L.I_{bias}}{k'W}} \quad 5.21$$

$$V_{dimin} = -V_{dimax} = -(V_{i1} - V_{i2}) \quad 5.22$$

5.5 Maximum and Minimum Differential Output Voltage

The large signal swing limitations of the output are also of interest. In this case, the swing limitations will be based on keeping both M_2 and M_4 in saturation. When V_{GS1} is taken above V_{GS2}, the output voltage, V_{OUT}, increases. Therefore,

$$V_{OUT(max)} = V_{DD} - V_{SD4,sat} \quad 5.23$$

$$= V_{DD} - (V_{SG3} - V_{thp,4}) \quad 5.24$$

$$= V_{DD} - \left(\sqrt{\frac{2I_{D1}}{\frac{Wk'}{L}}} + V_{thp,3} \right) + V_{thp,4} \quad 5.25$$

$$= V_{DD} - \left(\sqrt{\frac{I_{bias}}{\frac{Wk'}{L}}} \right) \quad 5.26$$

Minimum output voltage is determined by voltage on the gate of M_2

$$V_{OUT(\max)=} V_{I2} - V_{thn,2} \quad 5.27$$

5.6 Simulation Results:

The design parameters are given as follows:

Positive supply voltage = +4V

Negative supply voltage = -4V

W/L ratio of driver transistors (M_1 & M_2) = 2,

W/L ratio of load transistors (M_3 & M_4) = 2,

Input bias voltage = 2V,

Input voltage signal level = 10mV,

Biasing current source = 100μA,

Load capacitance = 0.05pF.

5.6.1. Transient Analysis:

The transient analysis of CMOS differential amplifier with current mirror load shows that output voltage signal is in same phase and amplified version of input voltage signal as shown in figure 5.4 and figure 5.5. Where V_{in} is 10mV (p-p) and V_{out} is 950mV (p-p).

Theoretically $A_v = \frac{v_{out}}{v_{id}} = g_m(r_{ds2}||r_{ds4})$

$g_m = \sqrt{2\frac{W}{L}\mu_n C_{ox} I_D}$ =$\sqrt{2 * 2 * 90u * 50u}$ =0.134 μA/V

$r_{ds} = \frac{1}{I_D \lambda}$

$(r_{ds2}||r_{ds4})$ = (2MΩ||1MΩ)=0.66MΩ

A_v= 0.134 μA/V X 0.66MΩ =8.97 which approximately matches with the SPICE calculation.

5.6.2. Frequency Response:

3dB cut-off frequency of the differential amplifier is 470 kHz as shown in the figure 5.6 in which voltage gain is plotted against frequency.

Theoretically $f_H = \frac{1}{2\,\pi C_{Load} R_{out}}$

$= \frac{1}{2\pi * 0.5p * 0.66M} = 482\ kHz$ which approximately matches with SPICE calculation.

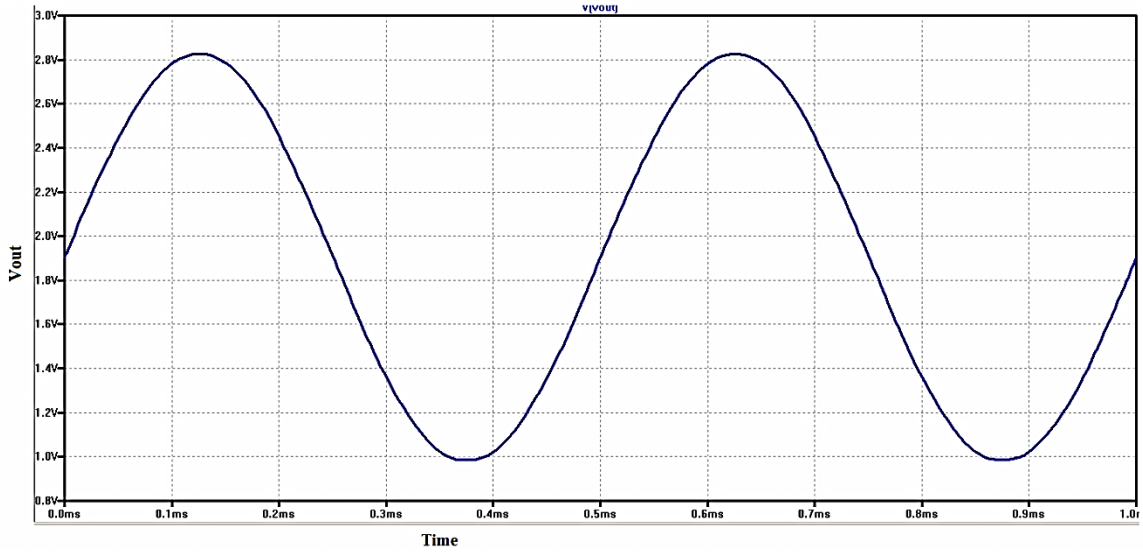


Figure 5.4 Transient response of input of Differential amplifier

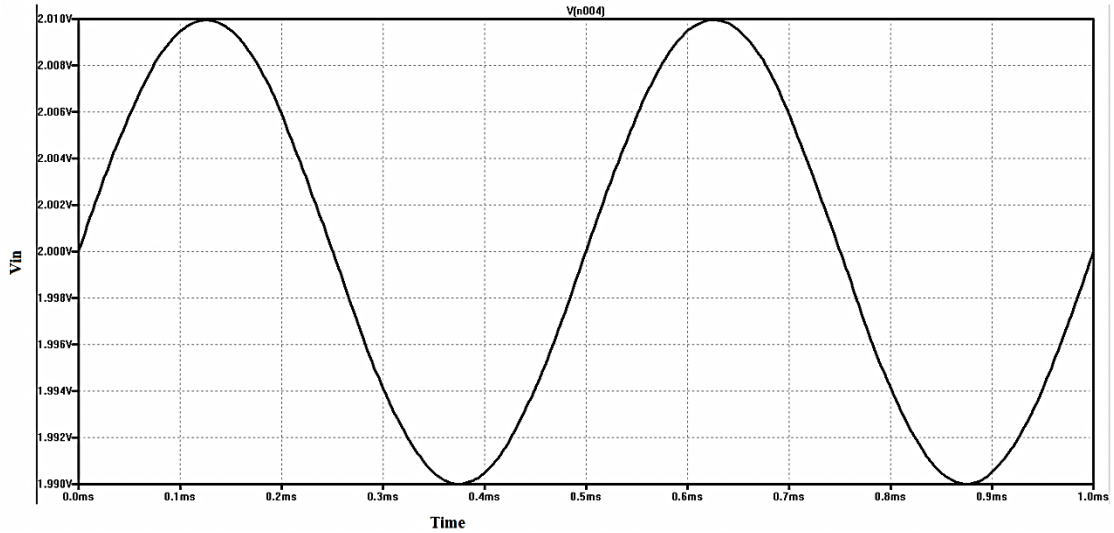


Figure 5.5 Transient response of output of Differential amplifier

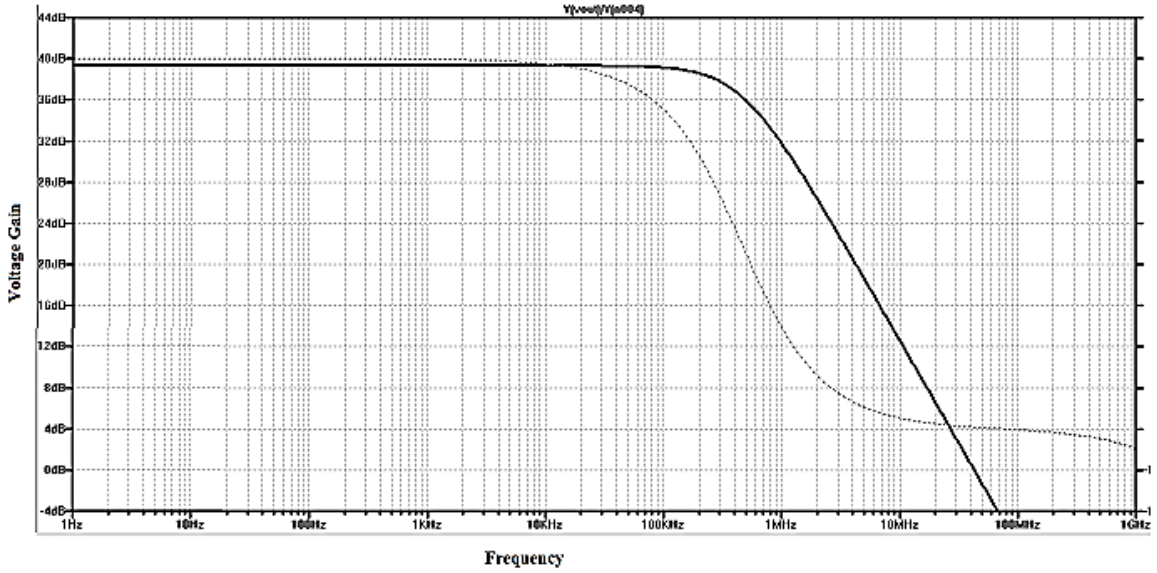


Figure 5.6 Frequency Response of Differential Amplifier

6. Summary

In this course work, Basics of Analog circuits which cover- MOSFET device, MOSFET biasing in different configurations, MOSFET amplifiers, small signal model for low frequency and high frequency, Amplifier parameters like gain, output and input resistances, frequency responses of common source, common drain and common gate amplifiers, Differential amplifiers, Negative feedback, Voltage controlled Voltage source, Voltage controlled Current source, Current controlled Voltage source, Current controlled Current source have been studied with the aid of video lectures on "Analogy Circuits" by Prof. Shanti Pavan IIT Madras.[6]

Later the focus has been shifted towards the design of integrated circuits. The difference in the philosophy of designing a system using discrete components and designing integrated circuits has been thoroughly understood. The modelling of MOSFET, passive devices like capacitor, resistors have been explored. Design of single stage amplifiers like common source amplifier, Cascode amplifier, Differential amplifier and their frequency responses have been studied in detail.

Simulation softwares give greater perspective of working principles of the circuits and design concepts. We have selected LT spice for simulating the circuits. LT spice is a free software with no limitations on its features and widely used in the academia, all over the world. Totally three integrated circuits- Common source with current mirror active load, Folded Cascode amplifier and differential amplifiers have been implemented in LT spice their frequency response have been explored.

Our research objectives are to design a LDO voltage regulator and improve its line and load regulation. To meet the above objective, we need a thorough knowledge about analog circuits, Integrated circuit design, in that especially design of amplifiers and differential pair which are very crucial for op-Amp design and finally good skill of using a simulation tool (in our case it is LT spice). In this regard this course work has really helped a lot in reaching the initial milestones of greater research path.

7.References

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[2] LT spice User Manual

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[4] Ms. Archana Y. Patil, Prof. S. B. Patil, “Distortion Analysis of Differential Amplifier”, IOSR Journal of Electronics and Communication Engineering (IOSR-JECE), Volume 6, Issue 6 (Jul. - Aug. 2013), PP 45-51.

[5] Bazes, M., Haifa, “Two novel fully complementary self-biased CMOS differential amplifiers”, IEEE Journal on Solid-State Circuits, Vol. 26 , Issue 2 , 06 August 2002.

[6]http://www.ee.iitm.ac.in/~nagendra/shanthi_lectures/EC201/31JulyEC201/31JulyEC201.html