Ph.D Course Work 02

on

Power Management Circuits

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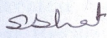**MANIPAL - 576 104**

CERTIFICATE

This is to certify that the report entitled "Power Management Circuit" submitted by Mr.Guruprasad (Reg No.140900006) is a bonafide report of the research course work carried out by him, and it is accepted as the course work-02 in partial fulfilment of the requirement for the award of the degree of Doctor of Philosophy.

Guide

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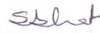Professor, Department of ECE, MIT

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Contents

List of Figures

List of Tables

1 Introduction

Power management broadly refers to the generation and control of regulated voltages required to operate an electronic system. It encompasses much more than just power supply design. Today's systems require power supply design be integrated with the system design in order to maintain high efficiency. In addition, distributed power supply systems require localized regulators at the PC board level, thereby requiring the design engineer to master at least the basics of both switching and linear regulators. Integrated circuit components such as switching regulators, linear regulators, switched capacitor voltage converters and voltage references are typical elements of power management.

Supplying and conditioning the power are the most fundamental functions of an electrical system. A loading application, be it a cellular phone, pager or wireless sensor node cannot sustain itself without energy and cannot fully perform its functions without a stable supply. The fact is that transformers, generators, batteries and other off line supplies incur substantial voltage and current variations across time and over a wide range of operating conditions. They are normally noisy and jittery not only because of their inherent nature but also because high power switching circuits like central-processing units (CPUs) and digital signal processing (DSP) circuits usually load it. These rapidly changing loads cause transient excursions in the supposedly noise free supply, the end results of which are undesired voltage droops and frequency spurs where only a dc component should exist. The role of the voltage regulator is to convert these unpredictable and noisy supplies to stable, constant, accurate and load independent voltages, attenuating these ill fated fluctuations to lower and more acceptable levels.

The regulation function is especially important in high performance applications where systems are increasingly more integrated and complex. A system on chip (SoC) solution, for instance, incorporates numerous functions, many of which switch simultaneously with the clock, demanding both high power and fast response times in short consecutive bursts. Not responding quickly to one of these load current transitions (i.e., load dumps) forces storage capacitors to supply the full load and subsequently suffer considerable transient fluctuations in the supply. The bandwidth performance of the regulator, that is, its ability to respond quickly, determines the magnitude and extent of these transient variations.

Regulators also protect and filter integrated circuits (ICs) from exposure to voltages exceeding junction breakdown levels. The requirement is more stringent and acute in emergent state of the art technologies whose susceptibility to breakdown voltages can be less than 2 V. The growing demand for space efficient, single chip solutions which include SoC, system in package (SiP), and system on package (SoP) implementations, drives process technologies to finer photolithographic and metal pitch dimensions. Unfortunately, the maximum voltage an IC can sustain before the onset of a breakdown failure declines with decreasing dimensions and pitch because as the component density increases, isolation barriers deteriorate.

References, like regulators, generate and regulate accurate and stable output voltages that are impervious to variations in the input supply, loading environment and various operating conditions. Unlike regulators, however, references do not supply substantial dc currents. Although a good reference may shunt positive and negative noise currents, its total load current reach is still relatively low. In practice, references supply up to 1 mA and regulators from 5 mA to several amps.

Historically, the standard for supply voltages was $\pm 15V$. In recent years the trend is towards lower supply voltages. This is partially due to the processes used to manufacture

integrated circuits. The transistor size is reduced drastically so one can put a large number of devices in a small area. These smaller feature sizes imply lower breakdown voltages, which, in turn indicate lower supply voltages.

Reduction in the supply voltage has the very desirable effect of reducing the power dissipation of digital circuits. However lowering the supply of linear circuits limits the dynamic range of the signal and lowering the signal swing by lowering the supply voltage does not imply that the noise level will be reduced by the same amount.

2 Classification of Voltage Regulators

A voltage regulator is normally a buffered reference that is a bias voltage cascaded with a non inverting op amp capable of driving large load currents in shunt-feedback configuration. Voltage regulators are generally classified as linear or switching. Linear regulators linearly modulate the conductance of a series pass switch connected between an input dc supply and the regulated output to ensure the output voltage is a predetermined ratio of its bias reference. Since the current flow and its control are continuous in time, the circuit is linear and analog in nature and because it can only supply power through a linearly controlled series switch, its output voltage cannot exceed its unregulated input supply.

A switching regulator is the counterpart to the linear solution and because of its switching nature, it can accommodate both alternating current (ac) and direct current (dc) input and output voltages, which is why it can support ac-ac, ac-dc, dc-ac, and dc-dc converter functions. Within the context of ICs, however, dc-dc converters predominate because the ICs derive power from available dc batteries and off line ac-dc converters and most loading applications in the IC and outside of it demand dc supplies to operate. Nevertheless, given its ac-dc converting capabilities, switching regulators are also termed switching converters, even if only dc-dc functions are performed.

From a circuit perspective, the driving difference between linear and switching regulators is that the latter is mixed-mode with both analog and digital components in the feedback loop. The basic idea in the switching converter is to alternately energize inductors and/or capacitors from the supply and de-energize them into the load, transferring energy via quasi lossless energy storage devices. To control the network, the circuit feeds back and converts an analog error signal into a pulse-width-modulated (PWM) digital pulse train whose on-off states determine the connectivity of the aforementioned switching network. From a signal processing perspective, the function of the switching network is to low pass filter the supply level swings of the digital train down to a milli volt analog signal, the average of which is the regulated output.The difference between linear and switching regulators are listed in table 1 [1].

3 Performance Parameters of Voltage Regulators

This section describes performance parameters of a voltage regulator such as dropout voltage, quiescent current, efficiency, transient response, line and load regulation, power supply rejection, output noise voltage, accuracy, and power dissipation [2].

Table 1: Difference between Linear regulator and Switched regulator

Linear Regulator	Switching Regulator
Output range is limited	Output range is flexible
Simple circuit	Complex circuit
Low noise content	High Noise Content
Fast response	Slow Response
Limited power efficiency	High power efficiency
Good for low power applications	Good for high power applications

3.1 Dropout Voltage

This refers to Low Dropout regulators (LDO). Dropout voltage is the input to output differential voltage at which the circuit ceases to regulate against further reductions in input voltage; this point occurs when the input voltage approaches the output voltage. In the dropout region, the PMOS pass element is simply a resistor, and dropout is expressed in terms of its on-resistance R_{on}.

$$V_{dropout} = I_O R_{on} \tag{1}$$

Figure 1 shows the input/output characteristics of the TPS76733 3.3 V LDO regulator. The dropout voltage of the TPS76733 is typically 350 mV at 1 A. Thus, the LDO regulator begins dropping out at 3.65 V input voltage; the range of the dropout region is between approximately 2 V and 3.65 V input voltage. Below this, the device is non-functional. Low dropout voltage is necessary to maximize the regulator efficiency.
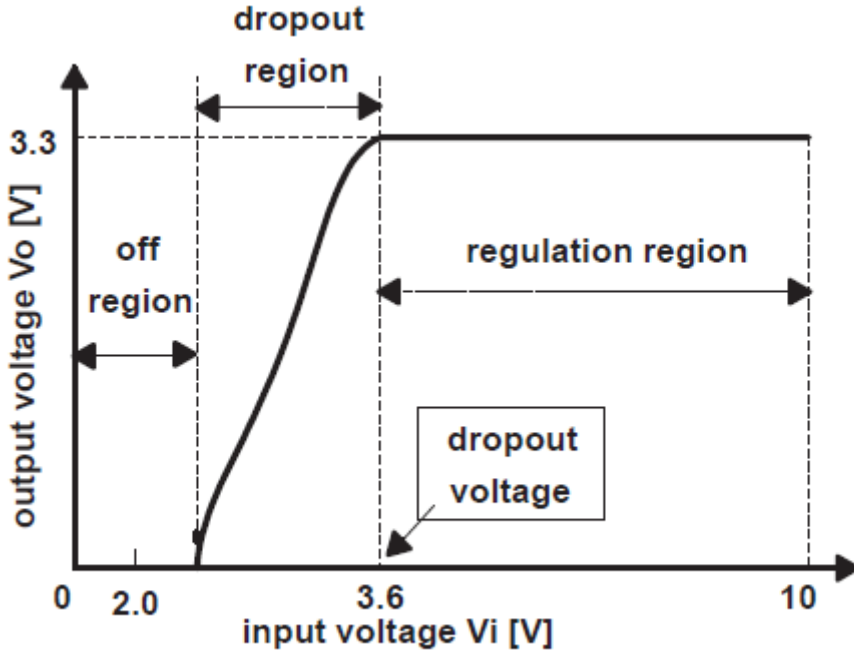

Figure 1: Dropout Region of TPS76733 (3.3 V LDO)

3.2 Quiescent Current

Quiescent or ground current is the difference between input and output currents. Low quiescent current is necessary to maximize the current efficiency. Figure 2 shows the quiescent current that is defined by

$$I_q = I_i - I_o \tag{2}$$

Quiescent current consists of bias current (such as band-gap reference, sampling resistor and error amplifier currents) and the gate drive current of the series pass element, which do not contribute to output power. The value of quiescent current is mostly determined by the series pass element, topologies, ambient temperature, etc. For bipolar transistors, the quiescent current increases proportionally with the output current, because the series pass element is a current-driven device. For MOS transistors, the quiescent current has a near constant value with respect to the load current since the device is a voltage-driven device. The only things that contribute to the quiescent current for MOS transistors are the biasing currents of band-gap, sampling resistor and error amplifier. In applications where power consumption is critical or where small bias current is needed in comparison with the output current, an LDO voltage regulator using MOS transistors is essential.
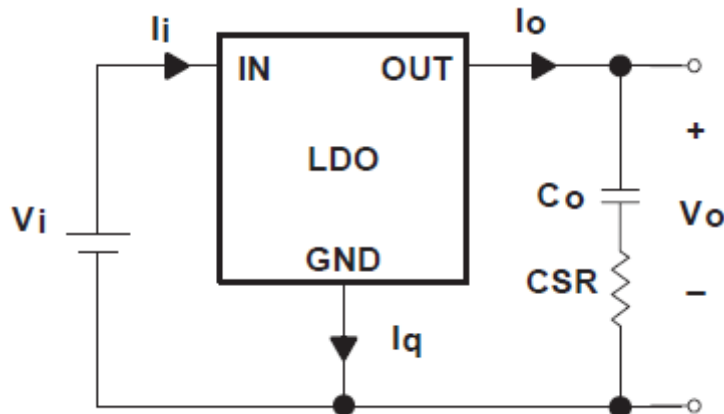

Figure 2: Quiescent Current in a Voltage Regulator

3.3 Efficiency

The efficiency of a regulator is limited by the quiescent current and input/output voltages as follows

$$efficiency = \frac{I_o V_o}{(I_o + I_q)V_i} 100 \tag{3}$$

To have a high efficiency, drop out voltage and quiescent current must be minimized. In addition the voltage difference between input and output must be minimized, since the power dissipation of LDO regulators accounts for the efficiency. The input/output voltage difference is an intrinsic factor in determining the efficiency, regardless of the load conditions.

3.4 Line Regulation

Line regulation is a measure of the circuit's ability to maintain the specified output voltage with varying input voltage. Line regulation is defined as

$$LineRegulation = \frac{\Delta V_o}{\Delta V_i} \tag{4}$$

Figure 3 shows the input voltage transient response of the TPS76933 3.3 V LDO regulator. A step change of input voltage was applied to the regulator, which is shown at the lower left in the figure. The resultant output voltage has been changed due to the different input voltages as shown in the right side of the figure. The line regulation is determined by $\Delta V LR_1$ and $\Delta V LR_2$ since line regulation is a steady-state parameter. Figure 4 shows the circuit performance of the TPS76933 LDO regulator with respect to the input voltages. The broken line shows the range of the output voltage variation ($\Delta V LR$) resulting from the input voltage change. Increasing open loop gain improves the line regulation.
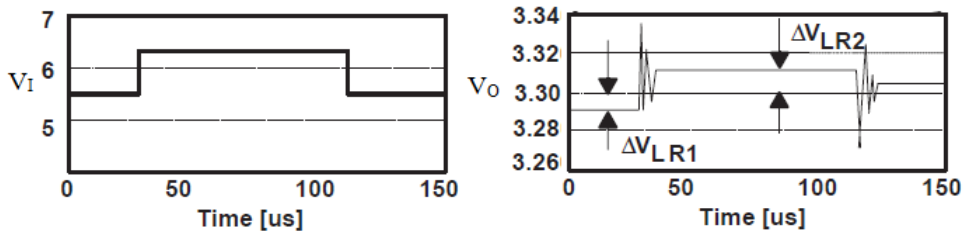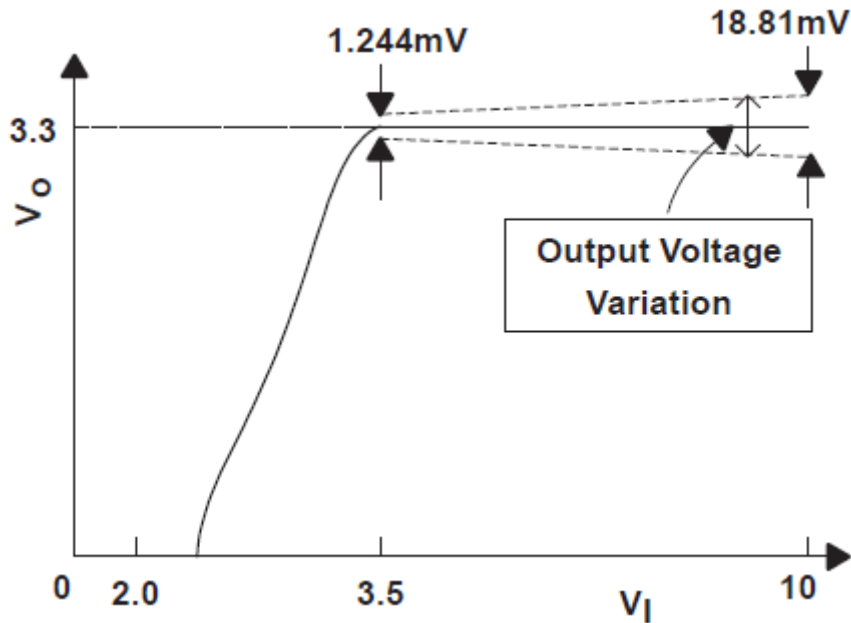

Figure 3: Input and Output Transient Response

Figure 4: Line Regulation of a Voltage Regulator

9

3.5 Transient Response

The transient response is the maximum allowable output voltage variation for a load current step change. The transient response is a function of the output capacitor value (C_{out}), the equivalent series resistance (ESR) of the output capacitor, the bypass capacitor (C_b) that is usually added to the output capacitor to improve the load transient response and the maximum load current ($I_{o,max}$). The maximum transient voltage variation is defined as follows

$$\Delta V_{tr,max} = \frac{I_{o,max}}{C_o + C_b}\Delta t_1 + \Delta V_{ESR} \tag{5}$$

where Δt_1 corresponds to the closed loop bandwidth of an LDO regulator, V_{ESR} is the voltage variation resulting from the presence of the ESR of the output capacitor. The application determines how low this value should be.

Figure 5 shows the transient response of a 1.2 V, 100 mA LDO regulator with an output capacitor of $4.7\mu F$. A step change of load current (near 90 mA) was applied to the regulator, which is shown in the upper trace of the figure. In the lower trace the output voltage drops approximately 120 mV and then the voltage control loop of the LDO regulator begins to respond to the step load change within $1\mu s$. The frequency bandwidth of the LDO regulator accounts for t1. Finally, the output voltage reaches a stable state within $17\mu s$. To obtain a better transient response, a higher bandwidth of the LDO regulator, higher values of output/bypass capacitors, and low ESR values are recommended.
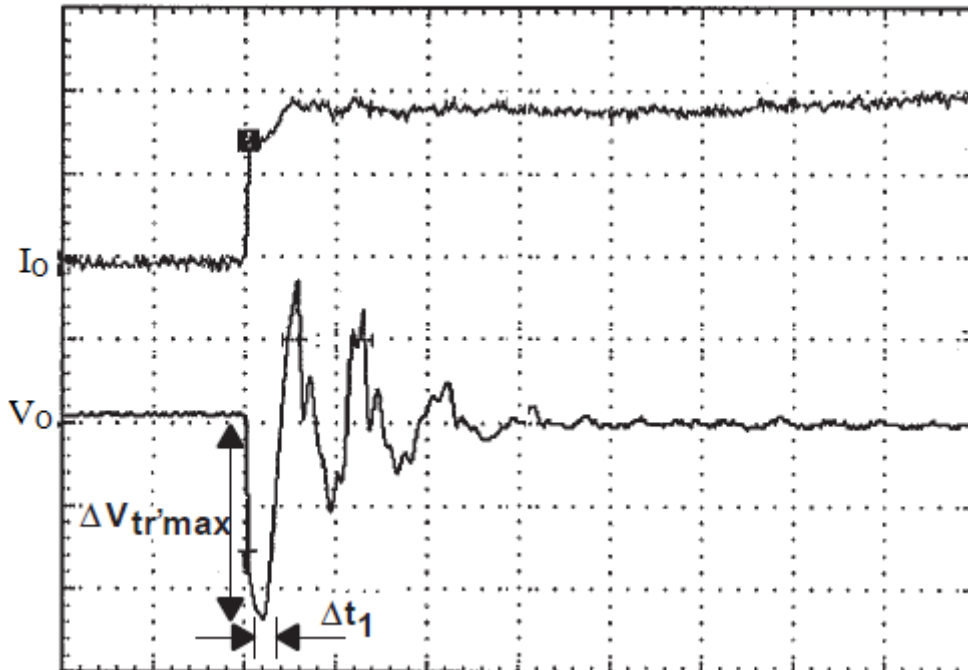

Figure 5: Transient Response of 1.2 V, 100 mA LDO Regulator

3.6 Load Regulation

Load regulation is a measure of the circuit's ability to maintain the specified output voltage under varying load conditions. Load regulation is defined as

$$loadregulation = \frac{\Delta V_o}{\Delta I_o} \tag{6}$$

The worst case of the output voltage variations occurs as the load current transitions from zero to its maximum rated value or vice versa, which is illustrated in Figure 6.
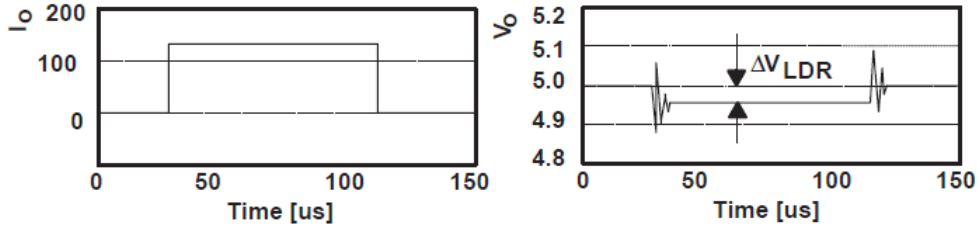

Figure 6: Load Transient Response of a Voltage Regulator

3.7 PSSR

The ripple rejection is defined by

$$PSSR = \frac{V_{o,ripple}}{V_{i,ripple}} \tag{7}$$

at all frequencies. The control loop tends to be the dominant contributor of supply rejection. Low ESR value, a large output capacitor, and added bypass capacitors improve the PSRR performance.

4 Linear Voltage Regulator

In this section, starting from a simple Zener voltage reference to various complex voltage regulators are discussed and their improvements are highlighted.

4.1 Zener Regulator

Voltage regulators need a reference to operate. A Voltage Reference is a part or a circuit that provides a stable voltage when outside parameters, such as supply voltage or temperature vary. The most common voltage reference is the Zener diode. A Zener diode is a diode where the avalanche reverse breakdown behaviour has been optimized and quantified such that the diode can be operated safely in that region.
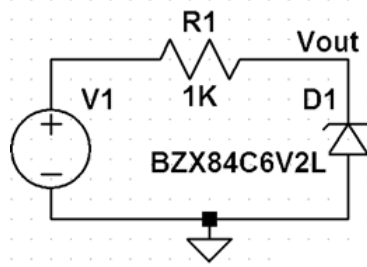
Figure 7: Zener Voltage Reference

The circuit shown in Figure 7 is simulated using LT spice to analyse the characteristic of a 6.2 V Zener diode BZX84C6V2L. Figure 8 shows the line regulation of above circuit. We can observe that in the range of -0.5 to about 6 V, the output voltage follows the input voltage. Below that, the Zener diode becomes forward biased and the voltage across it levels around -0.5 to -0.6 V, just like a regular diode. At source voltages above about 6 V, the Zener starts conducting current and the voltage across it levels around 6.2 V, which is the rated Zener voltage for that part.
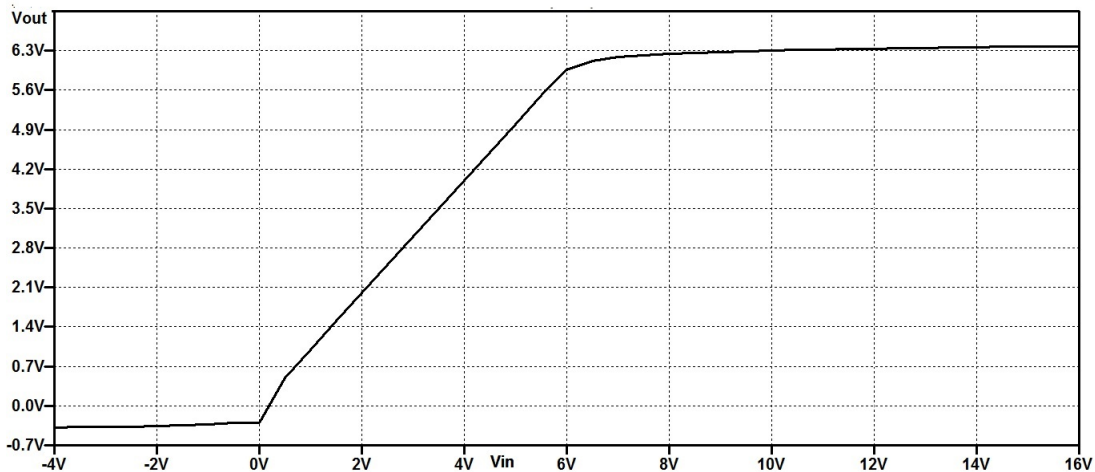

Figure 8: Line Regulation of Zener Regulator

In this case, the change in output voltage when the input voltage changes from 14 to 16 V (a 2 V change) is 20 mV, so the Line Regulation between 14 and 16 V is 0.01 as shown in Figure 8.

If we connect a load resistor R_L across Zener diode then the range load resistance in which Zener behaves as a voltage regulator is given by

$$R_{Lmin} = \frac{RV_z}{V_i - V_z} \tag{8}$$

$$I_{Lmin} = I_R - I_{ZM} \tag{9}$$

$$R_{Lmax} = \frac{V_z}{I_{Lmin}} \tag{10}$$

Where I_{ZM} is the maximum current through Zener without damaging the device. If we consider $V_{in} = 30V$, $V_Z = 6.2V$ and $R_1 = 1k\Omega$ then $R_{L,min} = 260\Omega$; $I_{L,max} = 23.8mA$; $I_{Lmin} = 5.8mA$; $R_{L,max} = 1.06k\Omega$. Figure 9 shows the load regulation of the the circuit. If
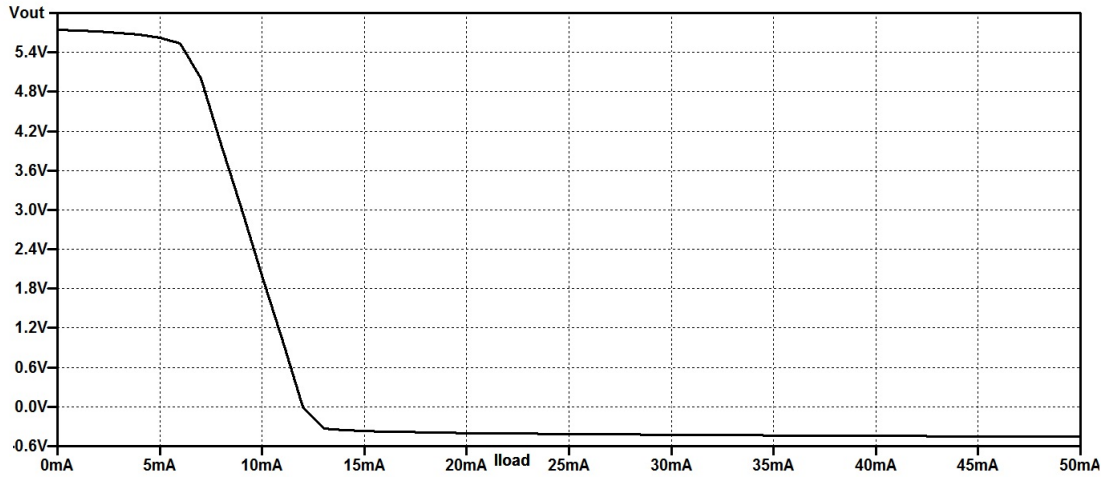
Figure 9: Load Regulation of Zener Regulator

we want to get more output current then we can consider one of the following techniques.

1. Reduce the value of R_1. We have seen that with the current value of 1 $k\Omega$, we would not reach the safe maximum power dissipation until the supply voltage is 24.2 V. We could reduce the value of R_1 so that the maximum safe power dissipation is reached at 18 V, which is the maximum supply voltage we need to design for.

2. Redesign the circuit with a higher power rated Zener (and decrease the value of resistor R_1 further to cause more current to flow through it), or

3. Add a current amplifier, using one or more transistor(s). Solution 1 is easy to implement and cost little, but it does not provide much of an improvement. In this case, the maximum Zener current is being 18 mA, that's also the maximum possible load current. In general, solution 2 does not make too much sense, because higher power Zener are harder to get and the circuit quickly would waste a lot of energy. With the trend for battery operated equipment, it is important to be familiar with solutions that do not waste power. Solution 3 is a little more complex, but offers more flexibility and is more efficient.

4.2   Linear Regulator Using a Pass Transistor

Figure 10 shows a linear Voltage regulator using a npn transistor for producing more output current. the transistor we added to the shunt regulator is in a configuration known as Emitter-Follower. That means the voltage on the emitter follows the voltage on the base (with a small offset typically of 0.6 to 0.7 V). The voltage gain of such a circuit is slightly less than 1. So, if the base voltage is maintained at 5.6 V, the voltage on the emitter will be about 4.9 to 5.0 Volts [3].
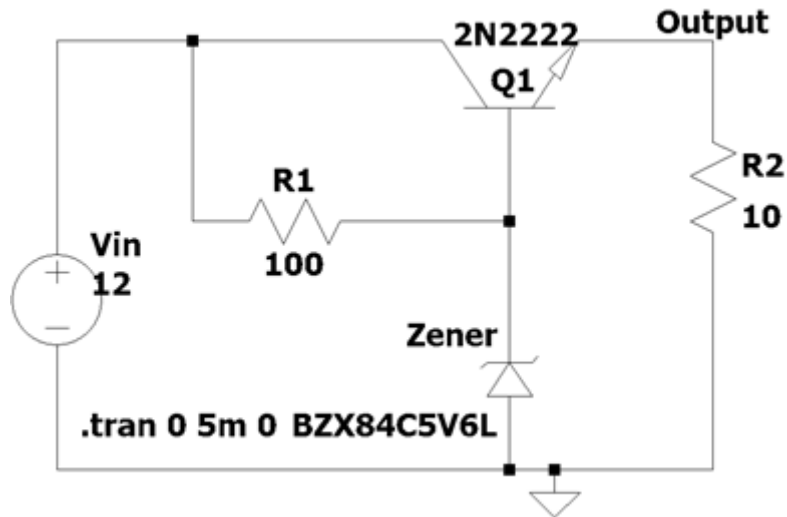
13

Figure 10: Linear Regulator Using a Pass Transistor

Figure 11 shows the line regulation of the above regulator. When V_{in} is varied from 8 V to 12 V for a 0.025 ms then V_{out} varies 0.1 V after reaching steady state.
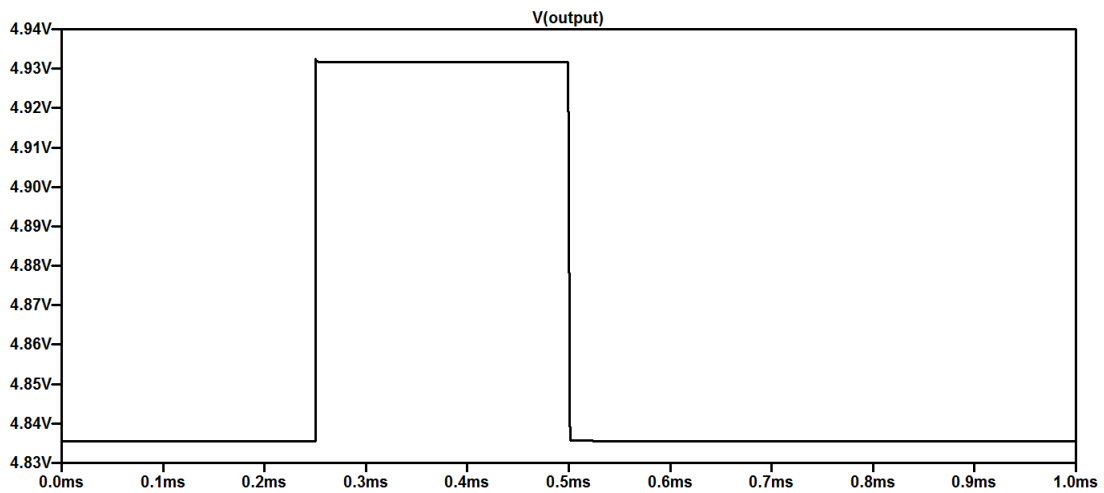

Figure 11: Line Regulation

Figure 12 shows the load regulation of the above voltage regulator. When load current is varied from 0 to 400 mA for 0.025 ms then there is steady state change of 0.45 V and an overshoot of 0.7 V and an under shoot of 2.86 V and it takes 1.87 μs to respond to change in the load.
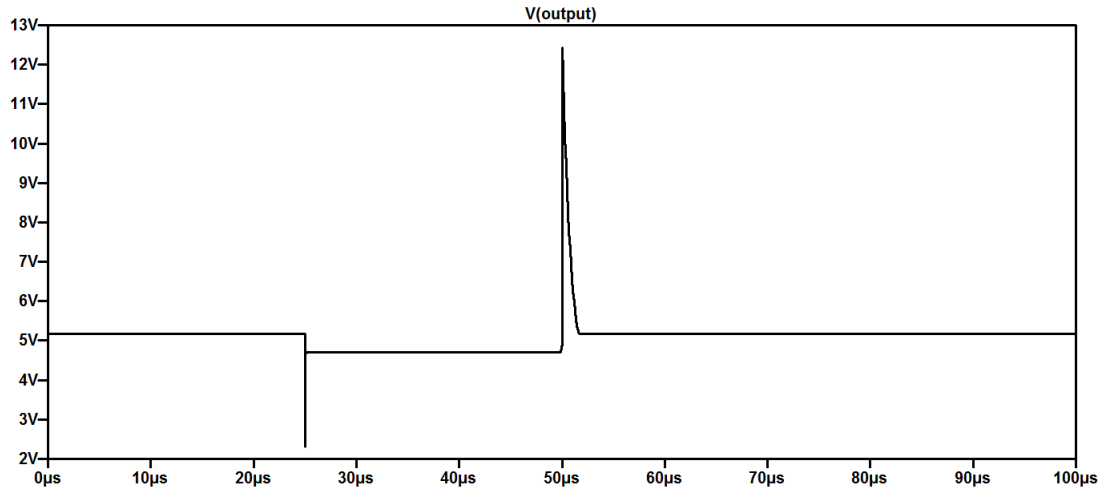
Figure 12: Load Regulation

When a 1 V AC signal ripple is applied over 12 V DC input to the above voltage regulator then we have obtained 30 mV ripple in the output as shown in figure 13.
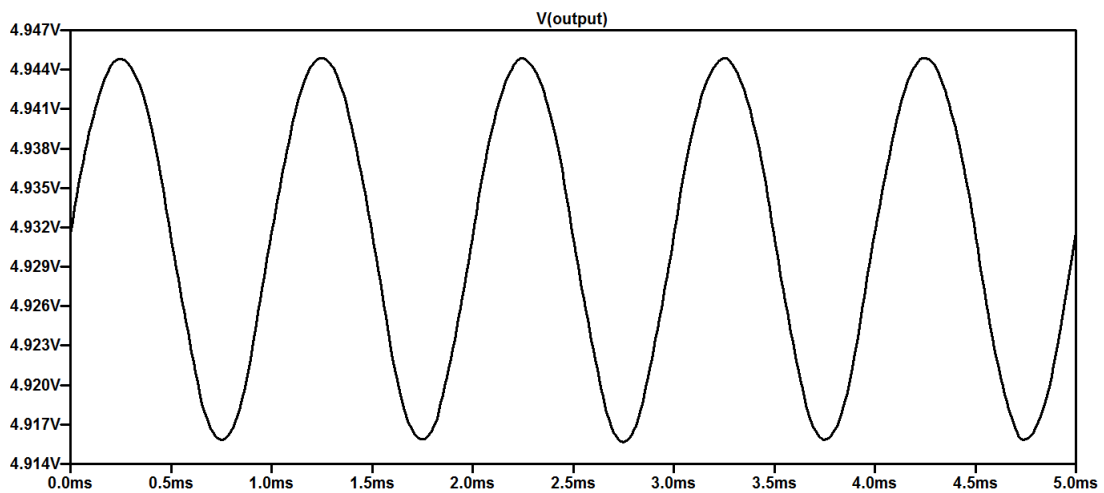

Figure 13: Output Ripple

4.3   An Improved Linear Regulator

The Load regulation of the previous regulator can be improved further by altering the architecture of the the regulator. For that we need a better output voltage control. Figure 14 shows the required architecture of regulator [3].
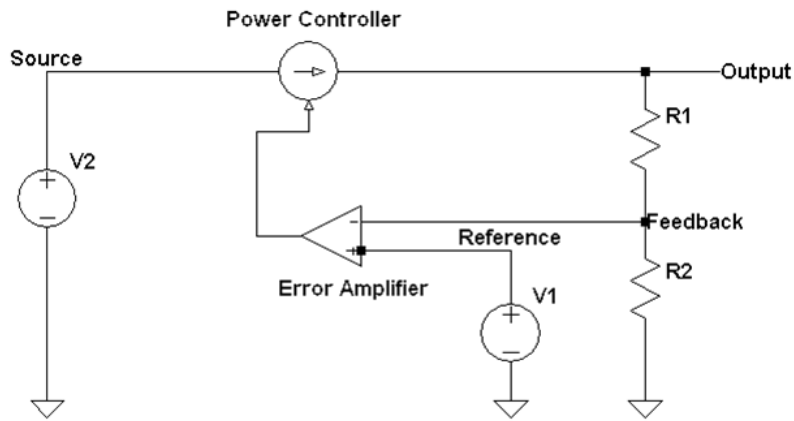
Figure 14: Voltage Regulator Architecture

In the previous regulator the error amplifier and power controller were same. It is better to separate the both. Figure 15 shows the modified voltage regulator.
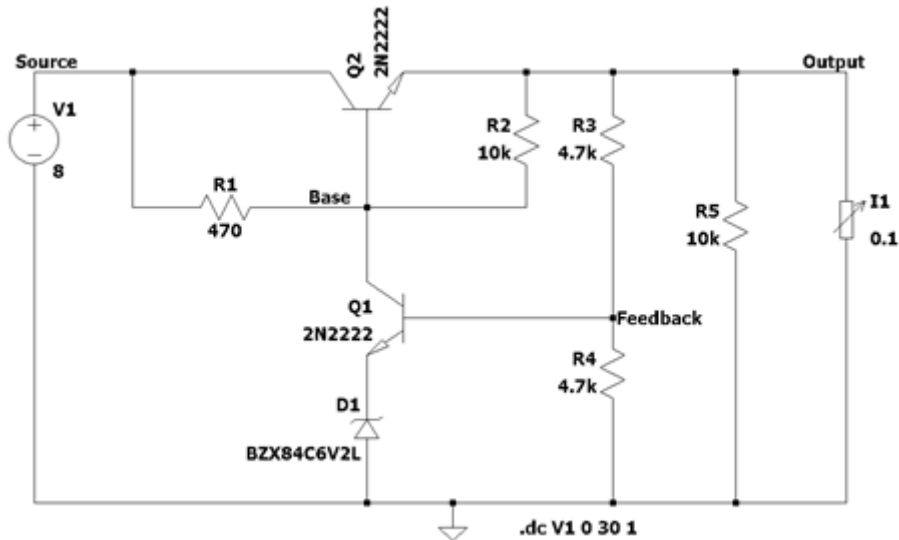

Figure 15: Modified Voltage Regulator

At power up, the output voltage is 0 V and the source voltage is ramping up. The voltage at the feedback point is the output voltage divided by two (because R_1 and R_2 are equal values), so it would be 0 V also. At that time, the voltage on Q_1's emitter does not matter because with 0 V on the base, Q_1 will be in cut-off (turned off), so it will not draw any collector current, so all the current available from R_3 will go to Q_2's base, turning it on. As Q_2 turns on, the output voltage will rise. When the output voltage reaches 13.6 V, the voltage at the feedback point will be 13.6 / 2 = 6.8 V, so Q_1 will have 0.6 V between base and emitter and it will start to turn on. As Q_1 turns on, it will start drawing current through its collector, reducing the current available to drive Q_2's base. Eventually, the circuit will stabilize with about 0.7 V across Q_1's base-emitter junction, which should correspond to 13.8 V output voltage.

Figure 16 shows the load regulation of the regulator. When load is varied from 0 to

400 mA then there is 360 mV variation in the output voltage and it takes 0.24 μs to respond.
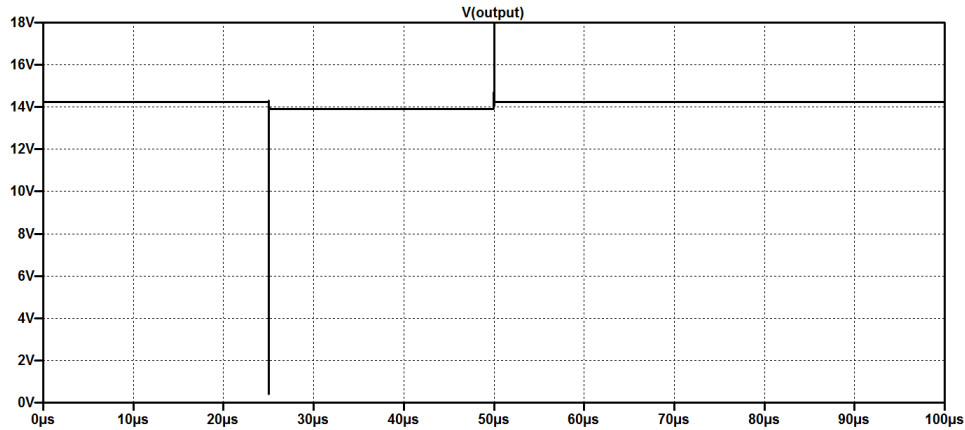

Figure 16: Load Regulation

Figure 17 shows the line regulation of above regulator. There is 0.5 V variation in steady state value when input voltage is varied from 16 V to 20 V.
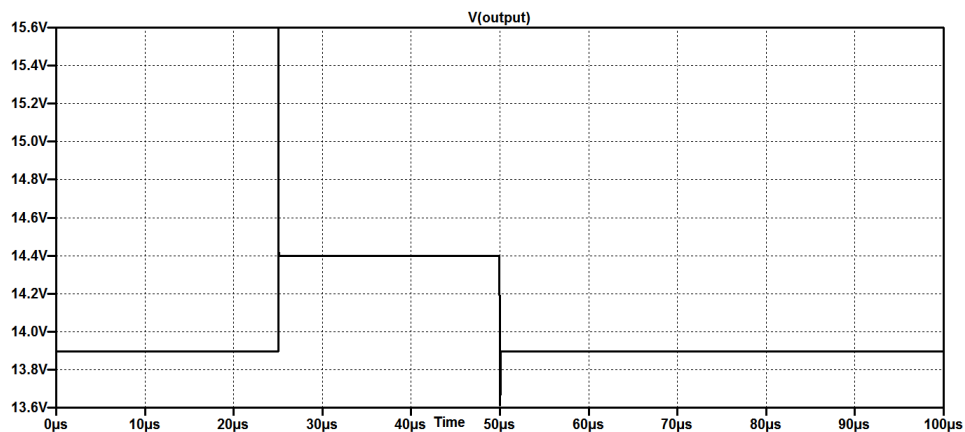

Figure 17: Line Regulation

4.4   Op-Amp Series Regulator

OP-Amp series Regulator uses Op-Amp as error amplifier as shown in Figure 18. The Op-Amp compares the Zener diode reference voltage with the feedback voltage from sensing resistors R_1 and R_2. If the output voltage varies, the conduction of transistor Q_1 is controlled to maintain the output voltage constant [3]. The output voltage will be maintained at a value of

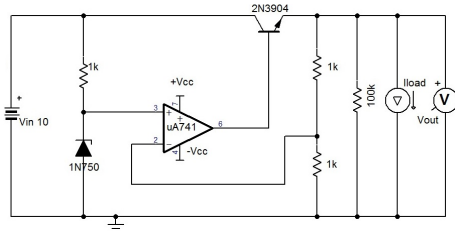$$V_o = (1 + \frac{R_1}{R_2})V_Z \tag{11}$$
$$V_o = 9.05V$$

Figure 18: OP-Amp Series Regulator

Line regulation of the above circuit is shown in Figure 19. Regulator will not work below V_{in} =10.48 V.
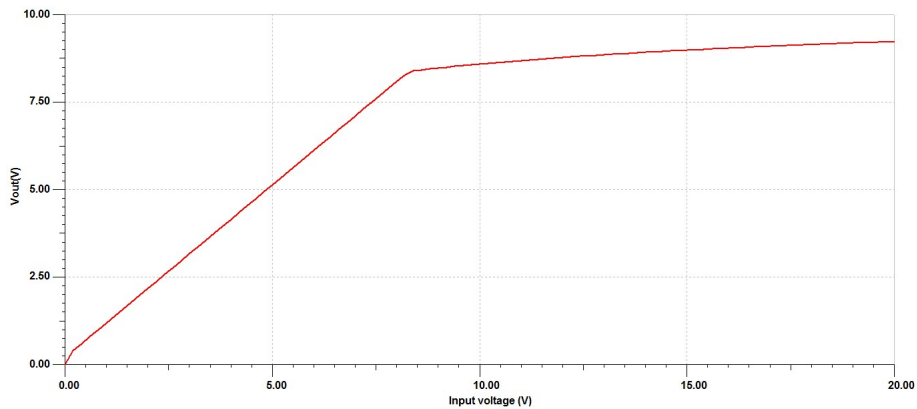

Figure 19: OP-Amp Series Regulator-Line Regulation

Load transient response is shown in figure 20 where load current is varied from 0 to 400 mA then there is undershoot of 2 V in the output voltage.
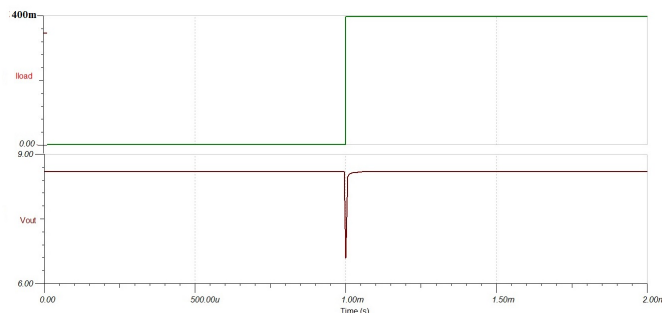

Figure 20: OP-Amp series Regulator Load Transient Response

4.5   Op-Amp Shunt Regulator

When load is connected in parallel with pass device then the regulator is called shunt regulator. The difference between shunt and series regulator is the former can supply more current and better accuracy. Reason is due to the Voltage controlled voltage source configuration of transistor in the series regulator can supply more current than the voltage

controlled current source configuration of transistor in shunt regulator. A shunt regulator using Op-amp is shown in Figure 21 where load is connected across pass device. Whenever output voltage changes, the error amplifier adjust its output accordingly so that difference at its inputs is nullified [3].
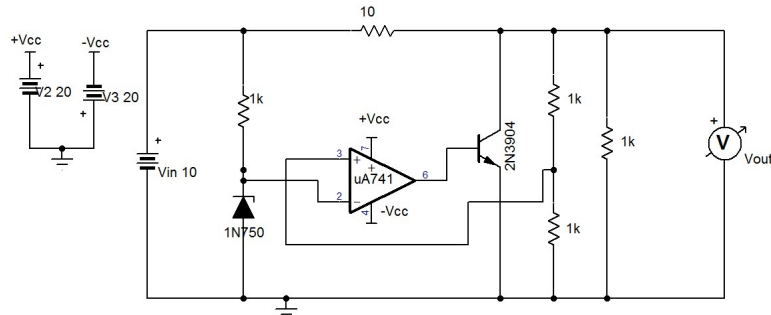

Figure 21: OP-Amp Shunt Regulator

Figure 22 shows line regulation of of shunt regulator at $I_{load} = 8.59$ mA.
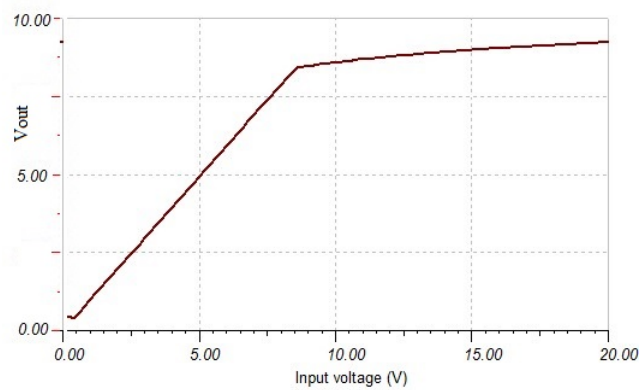

Figure 22: OP-Amp shunt Regulator Line Regulation

Figure 23 shows Load transient response of Shunt Regulator at $V_{in} = 10$ V. When I_{load} changes from 0 to 136 mA there is an undershoot of 90 mV in the output.
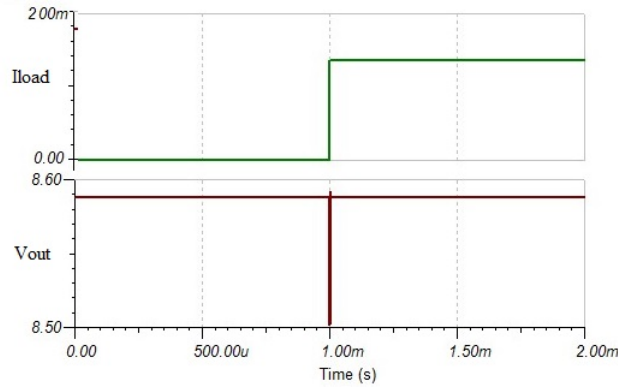
Figure 23: OP-Amp Shunt Regulator Load Transient Response

5 Pass Device

Pass device is a vital component in a linear voltage regulator. Precisely which type of pass device is chosen has a major influence on almost all major regulator performance issues. Most notable among these is the dropout voltage. Figure 24 shows the different possible types of pass devices used in voltage regulator architecture [4].

Figure 24: Different Pass Devices

Table 2 shows the pros and cons of different pass devices.

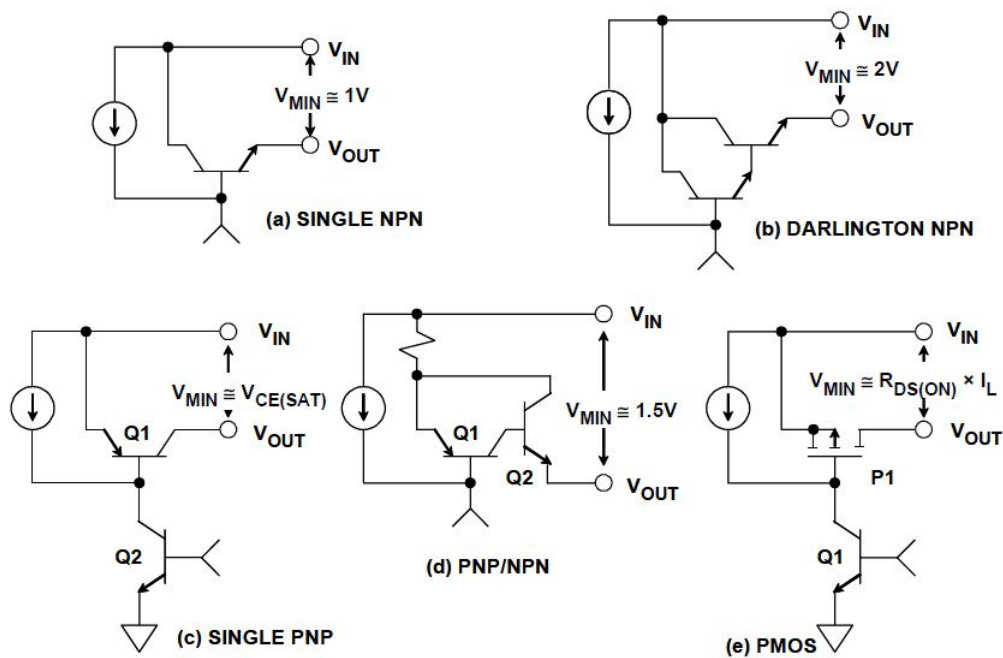Table 2: Pros and Cons of Different Pass Devices

Single NPN	Darlington NPN	Single PNP	PNP/NPN	PMOS
$V_{min} < 1V$	$V_{min} < 2V$	$V_{min} < -1V$	$V_{min} < 1.5V$	$V_{min} < 0.3V$
$I_L < 1A$	$I_L > 1A$	$I_L < 1A$	$I_L > 1A$	$I_L > 1A$
Follower	Follower	Inverter	Inverter	Inverter
Low Z_{out}	Low Z_{out}	High Z_{out}	High Z_{out}	High Z_{out}
Wide BW	Wide BW	Narrow BW	Narrow BW	Narrow BW

6 Switched Capacitor

This section examines switched capacitor voltage converters which accomplish energy transfer and voltage conversion using capacitors. The two most common switched capacitor voltage converters are the voltage inverter and the voltage doubler circuit shown in Figure 25. In the voltage inverter, the charge pump capacitor, C_1, is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle, its voltage is inverted and applied to capacitor C_2 and the load. The output voltage is the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle defined as the ratio of charging time for C_1 to the entire switching cycle time is usually 0.5, because that generally yields the optimal charge transfer efficiency[4].
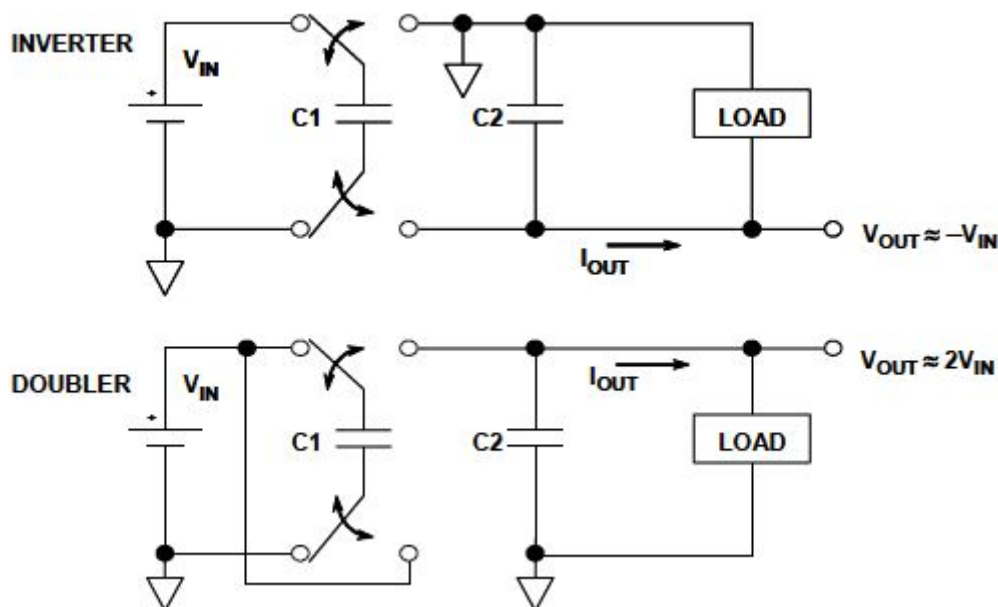

Figure 25: Basic Switched Capacitor Voltage Inverter and Doubler

After initial start up transient conditions and when a steady state condition is reached, the charge pump capacitor only has to supply a small amount of charge to the output

capacitor on each switching cycle. The amount of charge transferred depends upon the load current and the switching frequency. During the time the pump capacitor is charged by the input voltage, the output capacitor C_2 must supply the load current. The load current flowing out of C_2 causes a droop in the output voltage which corresponds to a component of output voltage ripple. Higher switching frequencies allow smaller capacitors for the same amount of droop. There are, however, practical limitations on the switching speeds and switching losses and switching frequencies are generally limited to a few hundred kHz.

The voltage doubler works similarly to the inverter; however, the pump capacitor is placed in series with the input voltage during its discharge cycle, thereby accomplishing the voltage doubling function. In the voltage doubler, the average input current is approximately twice the average output current.

6.1 Charge Transfer Using Capacitors

A fundamental understanding of capacitors (theoretical and real) is required in order to master the subtleties of switched capacitor voltage converters. Figure 26 shows the theoretical capacitor and its real-world counterpart. If the capacitor is charged to a voltage V, then the total charge stored in the capacitor, q, is given by q = CV. Real capacitors have equivalent series resistance (ESR) and inductance (ESL) as shown in the diagram, but these parasitics do not affect the ability of the capacitor to store charge. They can, however, have a large effect on the overall efficiency of the switched capacitor voltage converter [4].
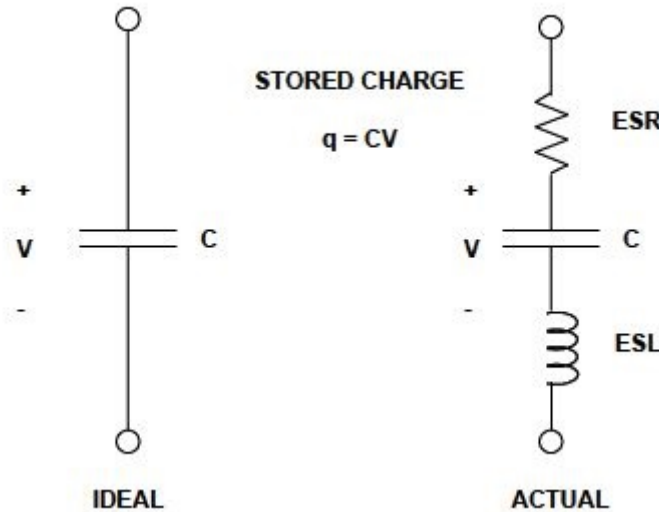

Figure 26: Stored Charge in a Capacitor

If an ideal capacitor is charged with an ideal voltage source as shown in Figure 27, the capacitor charge build up occurs instantaneously, corresponding to a unit impulse of current. A practical circuit will have resistance in the switch (RSW) as well as the equivalent series resistance (ESR) of the capacitor. In addition, the capacitor has an equivalent series inductance (ESL). The charging current path also has an effective series inductance which can be minimized with proper component layout techniques.
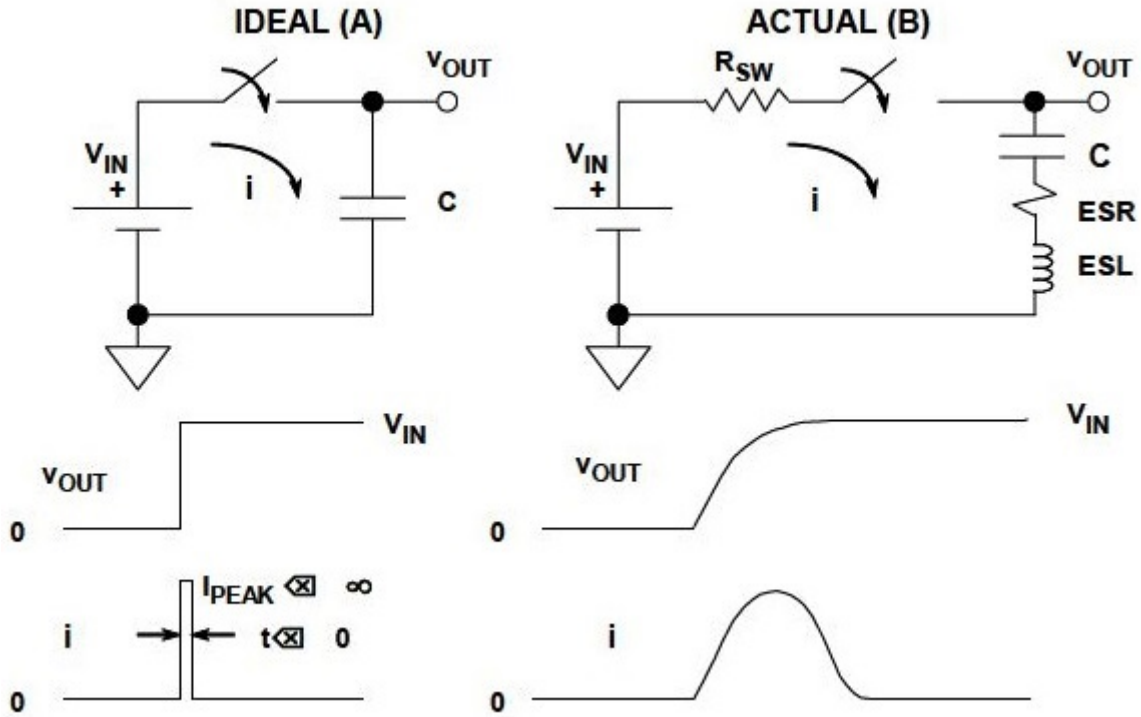
Figure 27: Charging a Capacitor from a Voltage Source

The law of conservation of charge states that if two capacitors are connected together, the total charge on the parallel combination is equal to the sum of the original charges on the capacitors. Figure 28 shows two capacitors, C_1 and C_2, each charged to voltages V_1 and V_2, respectively. When the switch is closed, an impulse of current flows, and the charge is redistributed. The total charge on the parallel combination of the two capacitors is $q_T = C_1.V_1 + C_2.V_2$. This charge is distributed between the two capacitors, so the new voltage, V_T, across the parallel combination is equal to $\frac{q_T}{(C_1+C_2)}$ or

$$V_T = \frac{q_T}{(C_1 + C_2)} = \frac{C_1.V_1 + C_2.V_2}{C_1 + C_2} = \frac{C_1}{C_1 + C_2}.V_1 + \frac{C_2}{C_1 + C_2}.V_2 \qquad (12)$$

This principle may be used in the simple charge pump circuit shown in Figure 28. Note that this circuit is neither a doubler nor inverter, but only a voltage replicator.
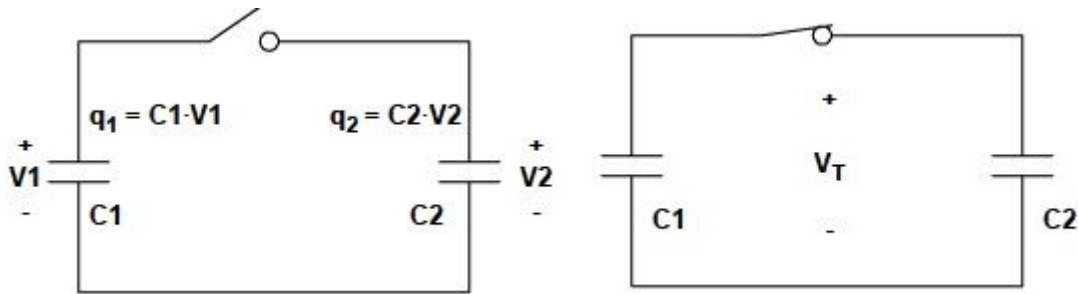

Figure 28: Charge Redistribution Between Capacitors

The pump charged to V_{IN}. When it is connected to C_2, the charge is redistributed and the output voltage is $V_{IN}/2$ (assuming $C_1 = C_2$). On the second transfer cycle, the output voltage is pumped to $V_{IN}/2 + V_{IN}/4$. On the third transfer cycle, the output voltage is pumped to $V_{IN}/2 + V_{IN}/4 + V_{IN}/8$. The waveform in Figure 29 shows how the output voltage exponentially approaches V_{IN}.
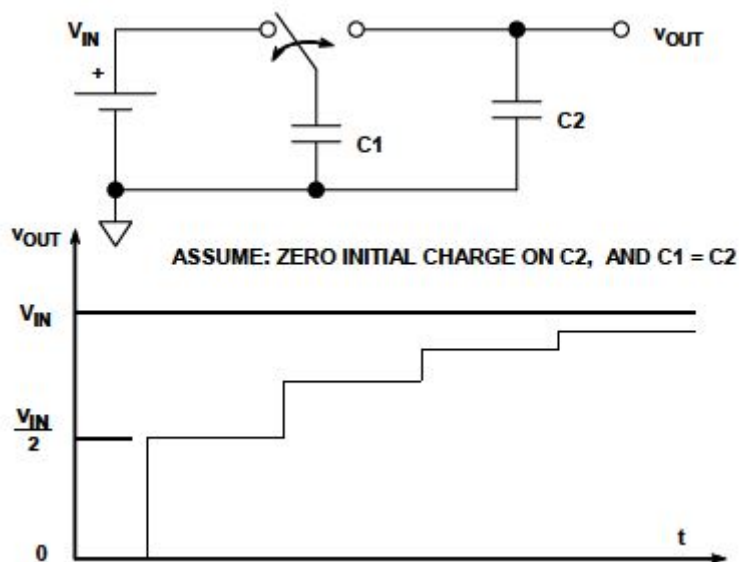

Figure 29: Continuous Switching

Figure 30 shows a pump capacitor, C_1, switched continuously between the source, V_1, and C_2 in parallel with the load. The conditions shown are after a steady state condition has been reached. The charge transferred each cycle is $\Delta q = C_1(V_1 V_2)$. This charge is transferred at the switching frequency, f. This corresponds to an average current (current = charge transferred per unit time) given by
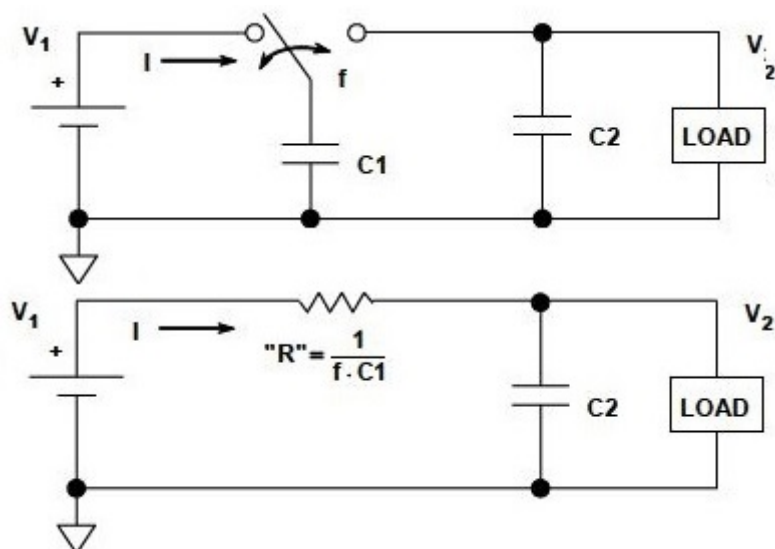

Figure 30: Continuous Switching, Steady State

24

$$I = f.\Delta q = f.C_1(V_1 - V_2) \tag{13}$$

$$I = \frac{V_1 - V_2}{\frac{1}{f}.C_1} \tag{14}$$

Notice that the quantity, $1/f.C_1$, can be considered an equivalent resistance, "R," connected between the source and the load. The power dissipation associated with this virtual resistance, "R," is essentially forced to be dissipated in the switch on resistance and the capacitor ESR, regardless of how low those values are reduced. It should be noted that capacitor ESR and the switch on-resistance cause additional power losses. In a typical switched capacitor voltage inverter, a capacitance of $10\mu F$ switched at 100 kHz corresponds to "R" $= 1\Omega$. Obviously, minimizing "R" by increasing the frequency minimizes power loss in the circuit. However, increasing switching frequency tends to increase switching losses. The optimum switched capacitor operating frequency is therefore highly process and device dependent. Therefore, specific recommendations are given in the data sheet for each device.

6.2 Unregulated Switched Capacitor Inverter Implementation

An unregulated switched capacitor inverter implementation is shown in Figure 31. The control circuit consists of an oscillator and the switch drive signal generators. The pump capacitor C_1, and the load capacitor C_2 are external. Not shown in the diagram is a capacitor on the input which is generally required to ensure low source impedance at the frequencies contained in the switching transients. The switches used in IC switched capacitor voltage converters may be CMOS or bipolar Transistors. Standard CMOS processes allow low on resistance MOSFET switches to be fabricated along with the oscillator and other necessary control circuits. Bipolar processes can also be used, but add cost and increase power dissipation.
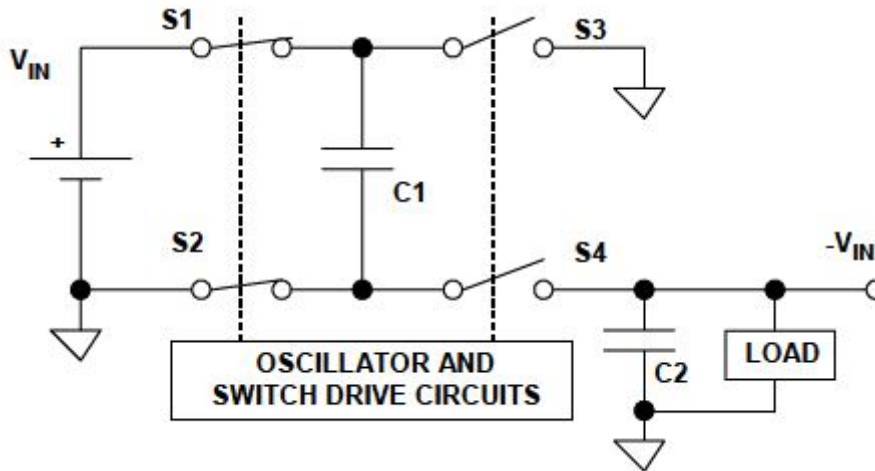

Figure 31: Switched Capacitor Voltage Inverter

6.3 Regulated Output Switched Capacitor Voltage Converters

Adding regulation to the simple switched capacitor voltage converter greatly enhances its usefulness in many applications. There are three general techniques for adding regulation to a switched capacitor converter. The most straightforward is to follow the switched capacitor inverter/doubler with a low dropout (LDO) linear regulator. The LDO provides the regulated output and also reduces the ripple of the switched capacitor converter. This approach, however, adds complexity and reduces the available output voltage by the dropout voltage of the LDO.

Another approach to regulation is to vary the duty cycle of the switch control signal with the output of an error amplifier which compares the output voltage with a reference. This technique is similar to that used in inductor-based switching regulators and requires the addition of a PWM and appropriate control circuitry. However, this approach is highly nonlinear and requires long time constants (i.e., lossy components) in order to maintain good regulation control.

By far the simplest and most effective method for achieving regulation in a switched capacitor voltage converter is to use an error amplifier to control the on resistance of one of the switches as shown in Figure 32, a block diagram of the ADP3603/ADP3604/ADP3605 voltage inverters. These devices offer a regulated 3 V output for input voltage of +4.5 V to +6 V. The output is sensed and fed back into the device via the V_{SENSE}pin. Output regulation is accomplished by varying the on resistance of one of the MOSFET switches as shown by control signal labelled "$R_{ON}CONTROL$" in the diagram. This signal accomplishes the switching of the MOSFET as well as controlling the on resistance [4].
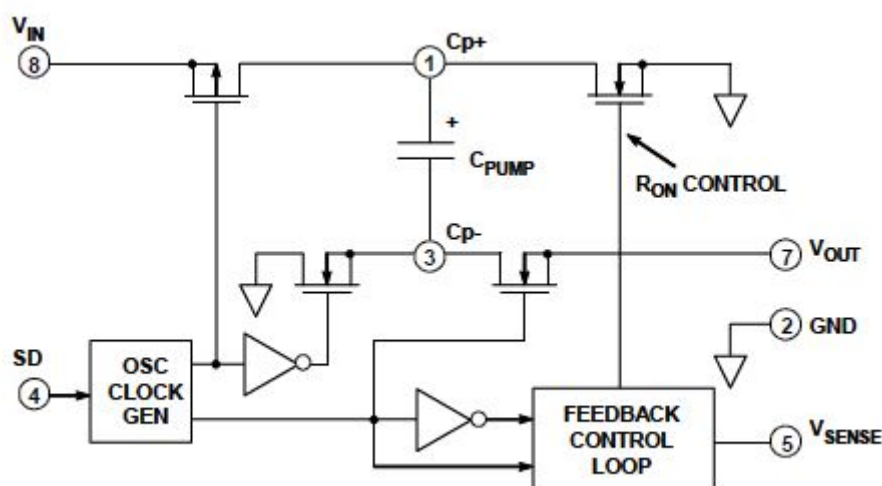

Figure 32: ADP3603/ADP3604/ ADP3605 Regulated 3 V Output Voltage Inverters

7 Design and Implementation of a Linear Voltage Regulator

This chapter describes the design and implementation of a 5 V linear voltage. A typical linear voltage regulator consists of error amplifier, pass device and feedback network. In
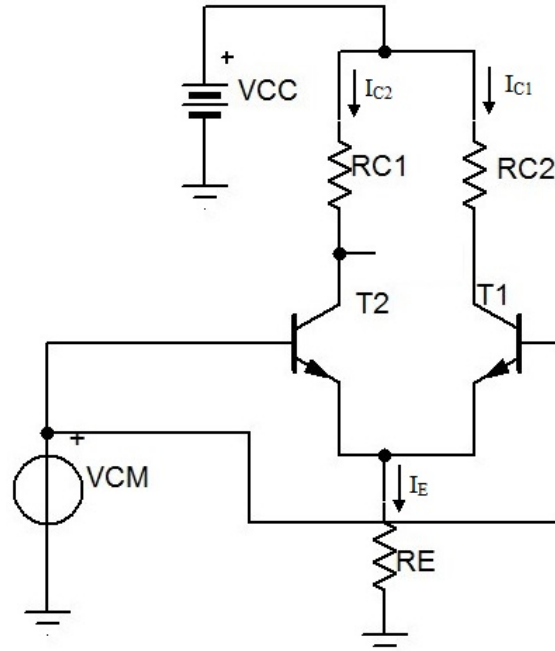
Figure 33: Differential Amplifier

our design a differential amplifier is used as error amplifier and is designed using BJTs as shown in Figure 33.

The bias condition assumes equal voltages at the base terminals of both transistors forcing the bias current I_E (set by R_E) to split equally between the transistors resulting in $I_{C1} = I_{C2}$. With $R_{C1} = R_{C2}$, equal voltages develop at the collector terminals of the both transistors.

Differential gain of Differential Pair is given by

$$A_d = \frac{R_C}{2r_e} = \frac{R_C.I_E}{2V_T} \tag{15}$$

If we would like to have gain=50 with I_E=1 mA then R_C=2.6 kΩ.

Proper biasing is required to keep the transistors in active region. Since I_E=1 mA, R_E can be found by following expression,

$$I_E = 1mA = \frac{V_E}{2R_E} = \frac{V_{cm} - 0.7}{2R_E}$$

Let $V_{cm} = 3V$ then R_E=1.15 kΩ

The single ended output voltage is given by

$$V_{o1} = V_{CC} - I_C.R_C \tag{16}$$

Let V_{CC}=9 V. So V_{o1}=6.4 V.

Since V_B=3 V,V_C=6.4 V and V_E=2.3 V transistors are in active region.

A DC analysis is conducted to check the DC operating point of all the nodes. Later a differential small signal 10 mV of frequency 10 kHz is applied and an AC analysis is carried out. Figure 34 shows frequency response of the differential amplifier. It offers

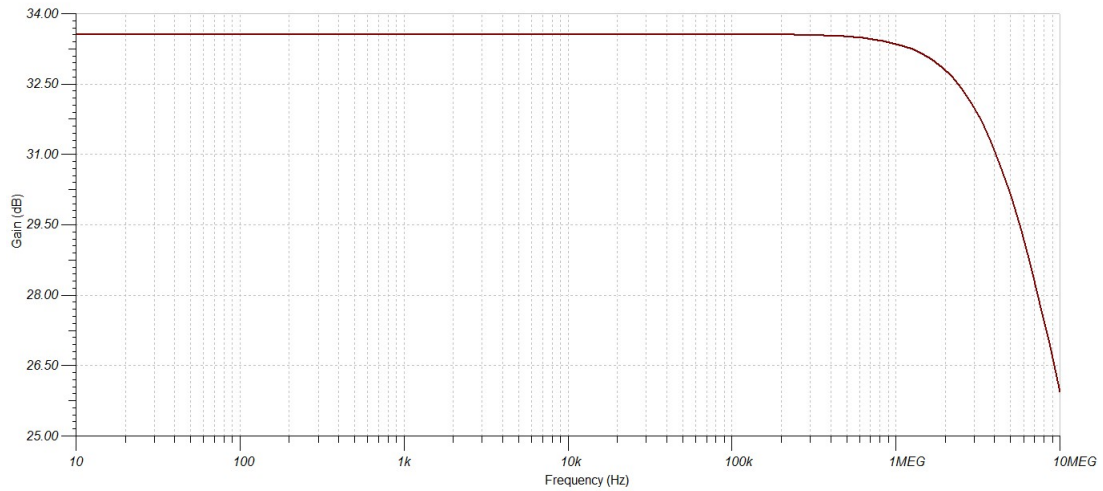approximately 50 dB gain. Figure 35 shows the transient response of the differential amplifier.

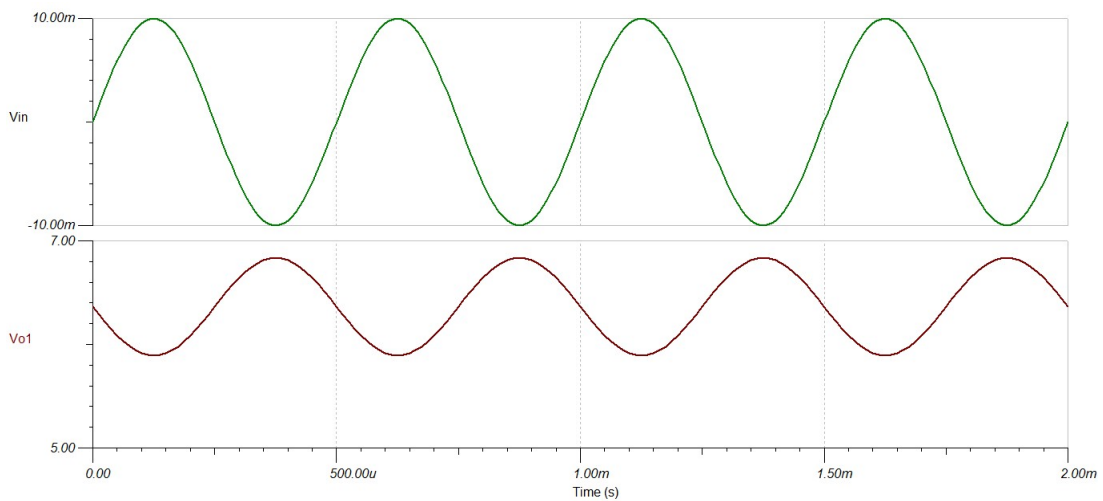Figure 34: Frequency Response of Differential Amplifier

Figure 35: Transient Response of Differential Amplifier

Figure 36 shows the differential amplifier with output buffer. Which not only boosts output current but also offers low output impedance.
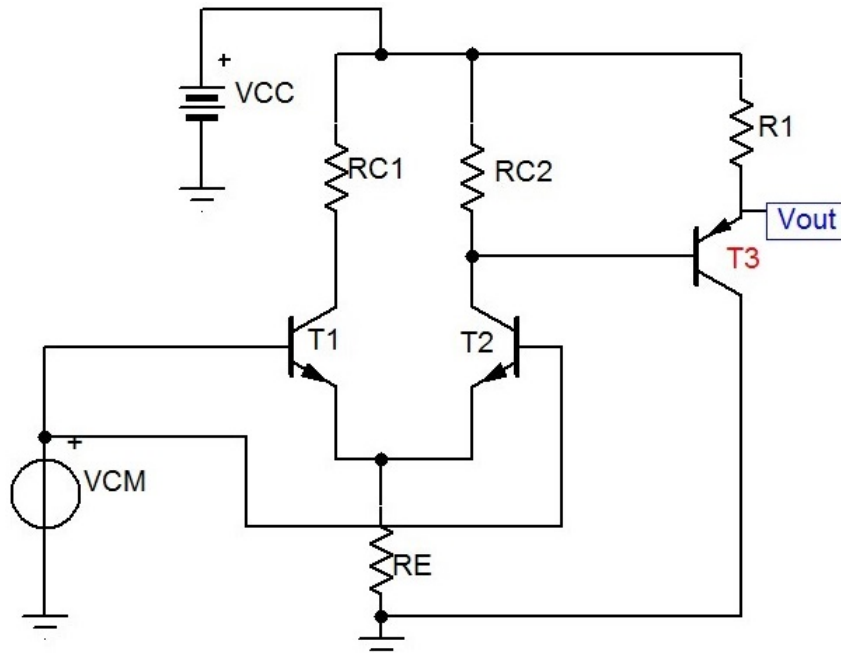
Figure 36: Differential Amplifier with Output Buffer

To design a linear regulator with V_{out}=5 V, a pass transistor is connected to the output of differential amplifier. A voltage divider network is used in the feedback network which connects the output terminal to the one of the inputs of differential amplifier. Since other input of differential pair is connected to 3 V, the loop always tries to keep voltage at the feedback point to 3 V.

In the voltage divider network, the voltage across R_2 is IR_2=3 V. Since we want 5 V output,

$$IR_1 + IR_2 = 5V$$

$$I = \frac{5}{R_1 + R_2}$$

since

$$IR_2 = 3V$$

$$R_2 = \frac{3}{2}R_1$$

If $R_1 = 1k\Omega$ then $R_2 = 1.5k\Omega$

Figure 37 shows the complete linear regulator with 5V output. Figure 38 shows the line regulation of the designed voltage regulator. Input voltage is varied from 0 V to 30 V at 10 mA load.

Figure 39 shows the load regulation of the designed voltage regulator. Load current is varied from 0 mA to 500 mA with $V_{in} = 9V$. The maximum possible load current till that circuit bahes as voltage regulator is 462 mA.
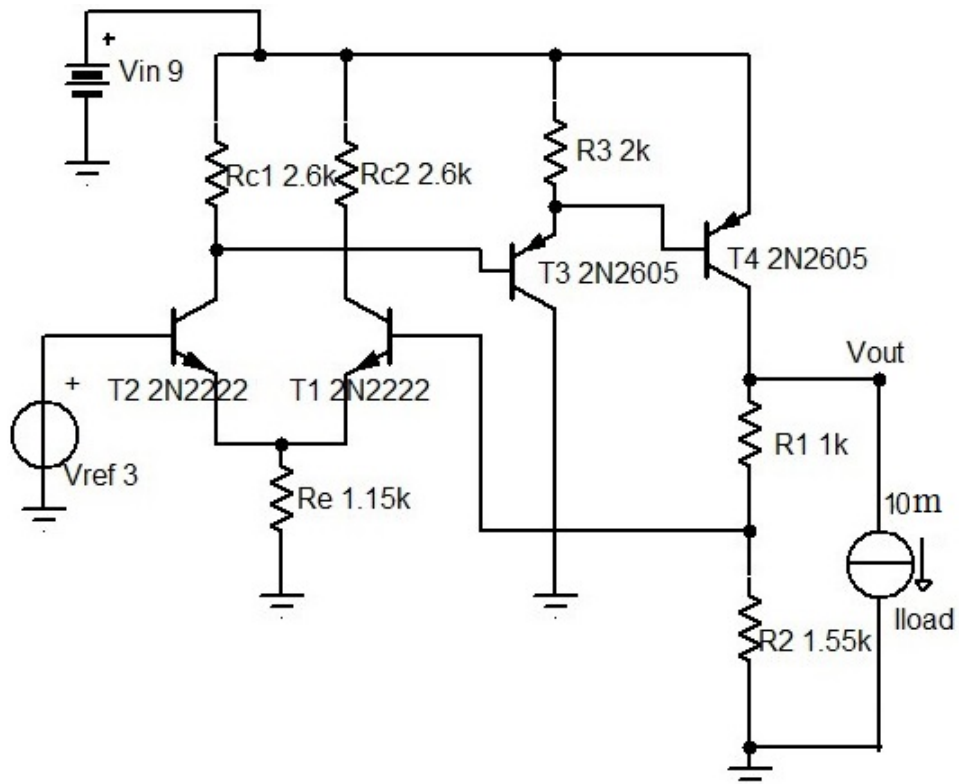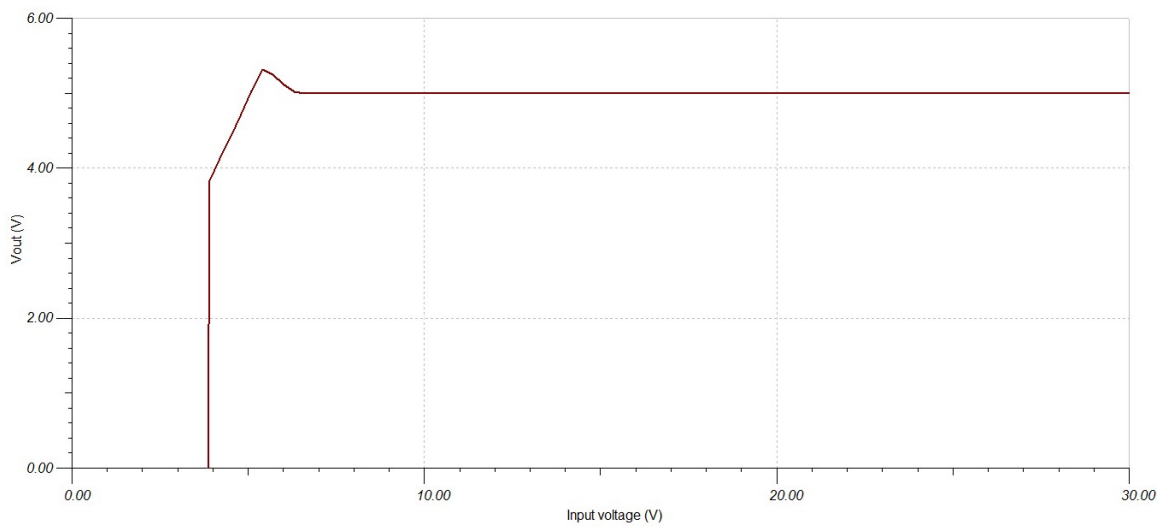
Figure 37: Linear Regulator

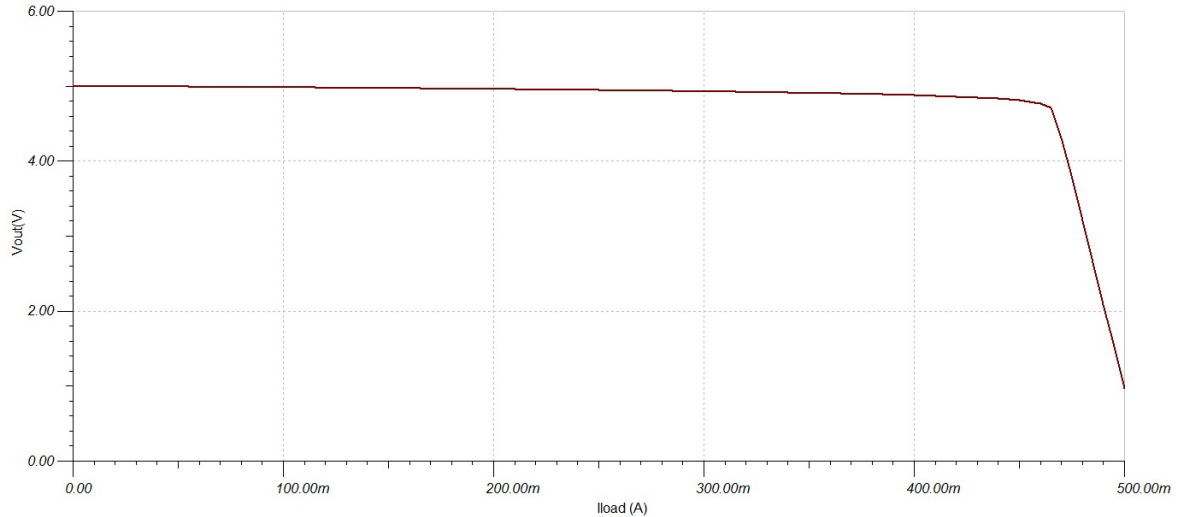Figure 38: Line Regulation of Linear Regulator

Figure 39: Load regulation of Linear Regulator

8   Summary

In this course work, basics of Power Management Circuits (PMC) have been studied thoroughly. Starting from the need of PMC, their classification namely linear regulator and switched regulators, performance parameters-dropout voltage, Efficiency, line regulation, load regulation, transient response, PSSR etc. have been investigated.

The characteristics of zener regulator, Regulator with pass transistor, Modified voltage regulator, Regulator using Op-Amps have been analysed. SPICE tool is used for the analysis. The significance of Pass devices have been studied.

In the later stage, the working principle of switched capacitor, Basics of voltage inverter and doubler, Regulation of voltage inverter and its characteristics have been studied.

Since the objective of our research is to design a low dropout voltage regulator which is a Power Management Circuit and improve its parameters, this course work has helped in this regard.

References

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[2] Texas Instrument, Understanding the Terms and Definitions of LDO Voltage Regulators, Application report, October 1999.

[3] Robert Boylestad and Louis Nashelsky, Electronic Devices and Circuit Theory, Prentice Hall, tenth edition, 2013.

[4] Analog Devices Company White papers.