Design of Common Source Amplifier

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Abstract

This article explains basic structure of common source amplifier and how to design it for a given specification. An example is taken to illustrate the design procedure and verified using LT spice tool.

Introduction

Common Source (CS) structure is the very basic form of an amplifier using MOSFETs. Though it is simple, it gives a decent gain - bandwidth product. Design of CS amplifier is first step for any analog circuit beginner. Figure 1 shows a typical structure of a common source amplifier.

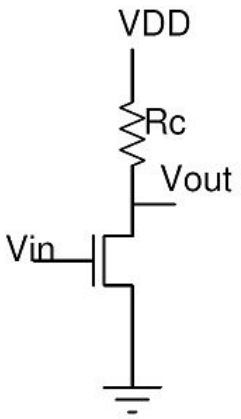

Figure 1: Typical structure of CS amplifier

however the gain depends on R_C resistor. To have a large gain, R_C must be large but large R_C makes VD smaller hence MOSFET may slip into triode region. So instead of Rc if we put a device which offers high resistance for small signal and low voltage drop for DC, we can achieve relatively large gain. We use a PMOS transistor in saturation region as an active load which offers high resistance for small signal and low voltage drop (V_{DS}) for DC.

Figure 2 shows the structure of CS amplifier with active load.

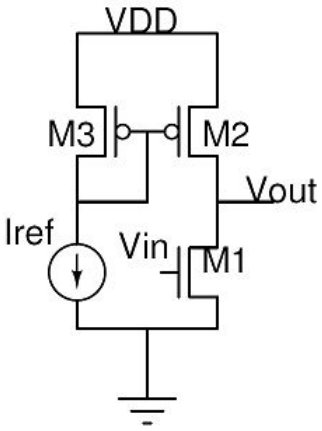

Figure 2: CS amplifier with active load

The active load is biased using current mirror technique. In the Figure 2. M_1 is the transistor in CS configuration, M_2 is active load and M_3 is a diode connected transistor which mirrors I_{ref} current into M_2 transistor. Since drain and gate of M_3 are tied together, it offers a good bias stability.

Figure 3 shows the small signal circuit of above mentioned CS amplifier.

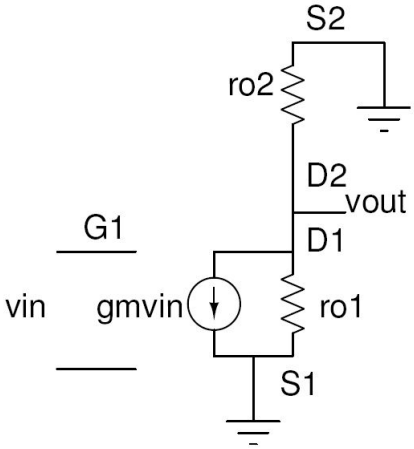

Figure 3: Small signal circuit of CS amplifier with active load

Gain of CS amplifier with active load can be found using following equations.

$$v_{out} = g_{m1} v_{in} * (r_{01} || r_{o2})$$

where g_{mx} is the transconductance of x^{th} transistor
r_{ox} is the output resistance of x^{th} transistor

$$v_{out} = \frac{2I_1}{V_{GS1} - V_{th}} v_{in} * \frac{r_{o1}}{2}$$

$$v_{out} = \frac{2I_1}{V_{GS1} - V_{th}} v_{in} * \frac{V_{A1}}{2I_1}$$

where V_A is the early voltage of transistor

$$Gain = \frac{v_{out}}{v_{in}} = \frac{V_{A1}}{V_{GS1} - V_{th}}$$

So gain is limited by device parameter V_A and over drive voltage (V_{ov}) $V_{GS1} - V_{th}$
Figure 4. shows the high frequency model of typical CS amplifier.

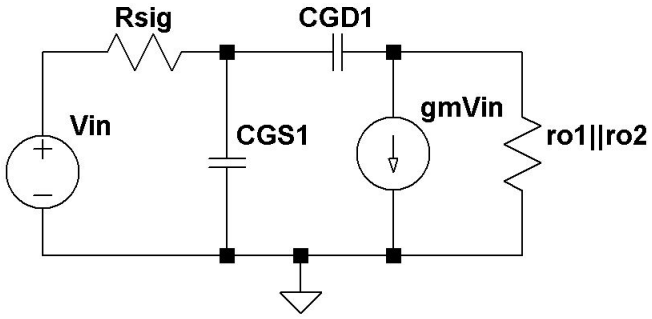

Figure 4: High frequency model of CS amplifier with active load

Using miller theorem, the floating capacitor C_{GD1} is split into two capacitors, one at the input side and another at the output side. Hence,

$$C_{in} = C_{GS1} + C_{GD1}[1 + g_{m1} * (r_{o1}||r_{o2})]$$

$$C_{out} = C_{GD1}$$

The CS amplifier has two poles

$$f_1 = \frac{1}{2\pi R_{sig} C_{in}}$$

$$f_2 = \frac{1}{2\pi r_{o1}||r_{o2} * C_{in}}$$

However f_1 is dominant pole and decides the bandwidth.

Design example

As an example, a CS amplifier is designed using 180 nm technology for a gain of 40 dB. Table 1 shows the technology parameters of 180 nm technology.

Table 1: 180 nm Technology parameters

Parameters	NMOS	PMOS
V_{th} $[V]$	0.4 V	-0.4 V
KP $[\mu A/V]$	210	52
LAMBDA $[V^{-1}]$	0.12	0.12

To achieve a gain of 40 dB i.e a gain of 100, a suitable overdrive voltage must be chosen. Since

$$Gain = \frac{V_{A1}}{V_{GS1} - V_{th}}$$
$$100 = \frac{7.9}{V_{GS1} - 0.4}$$
$$V_{GS1} = 0.079V$$

But this is too small, size of required M_1 will be too large. so we will keep overdrive voltage as 0.1 V. So gain will be 79.

The M_1 size is calculated from

$$I_1 = \frac{1}{2} K_P (\frac{W}{L})_1 V_{ov1}^2$$

If I_1 is taken as 50 μA

$$(\frac{W}{L})_1 = 48$$

In the current mirror part a resistor is connected in series with M_3 to produce 50 μA. If V_{D3} is set to 0.6 V i.e $V_{DS3} = V_{GS3}$=0.7V then size of M_3

$$I_3 = \frac{1}{2} K_P (\frac{W}{L})_3 (V_{GS3} - V_{th})^2$$

$$50\mu = \frac{1}{2} 51\mu (\frac{W}{L})_3 (0.7 - 0.4)^2$$

$$(\frac{W}{L})_3 = 23$$

Voltage across R_B is 0.6 V and current throug it is 50μA. Hence R_B is 13$k\Omega$

Size of M_2 and M_3 must be same to have same bias current.

The designed parameters are listed in table 2

Table 2: Device parameters

Parameters	Value
$(W/L)_1$	48
$(W/L)_2$	23
$(W/L)_3$	23
V_{DD}	1.3
I_{ref}	50μA
R_B	13$k\Omega$

The designed CS amplifier is simulated using LT spice. First dc operating point is calculated. Then a small signal is applied with 0.5V DC shift and magnitude response is plotted as shown in Figure 5. The obtained gain is 38.8 dB and bandwidth is 23 MHz.

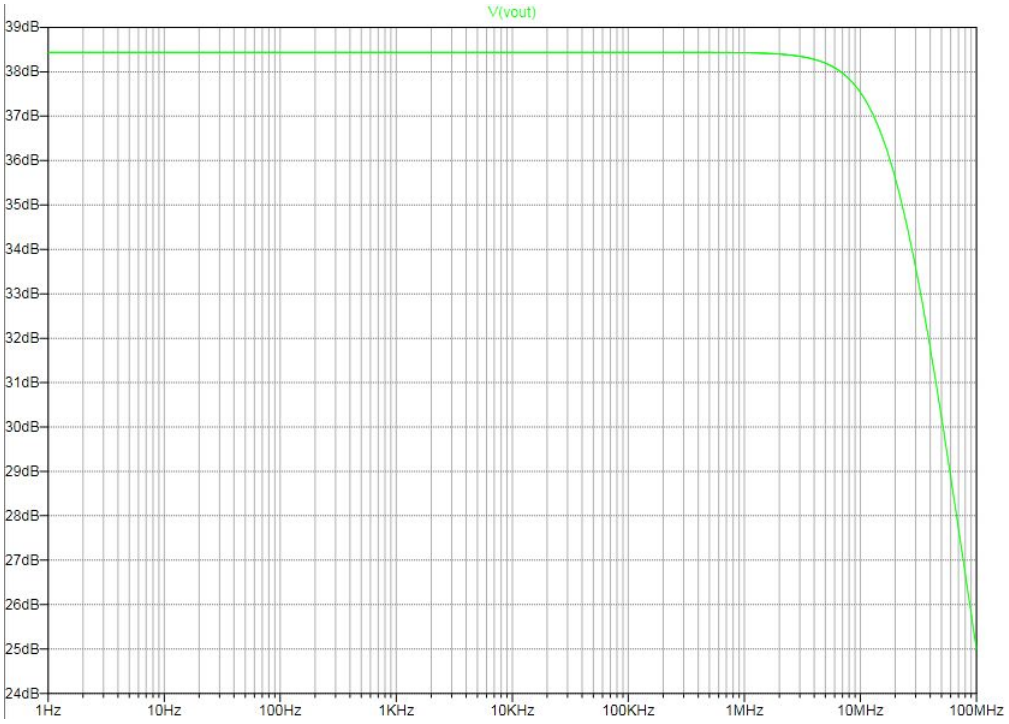

Figure 5: Frequency response of CS amplifier with active load

We have assumed source resistance as 0Ω. So if we consider source resistance as $1k\Omega$ the bandwidth will be reduced since dominant pole is dependent on R_{sig} and C_{in}. Figure 6 shows the frequency response of amplifier with source resistance of $1k\Omega$

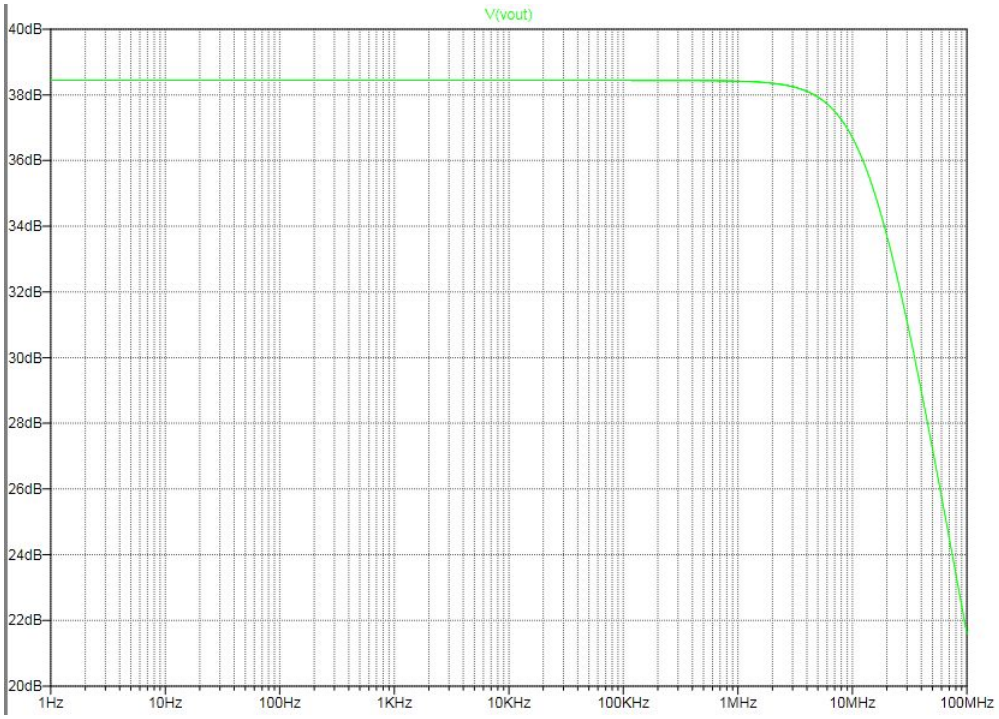

Figure 6: Frequency response of CS amplifier with active load

It can be seen that bandwidth is reduced to 14 MHz.

Lay out of the designed circuit is done using "MAGIC VLSI" tool which is shown on the below figure.

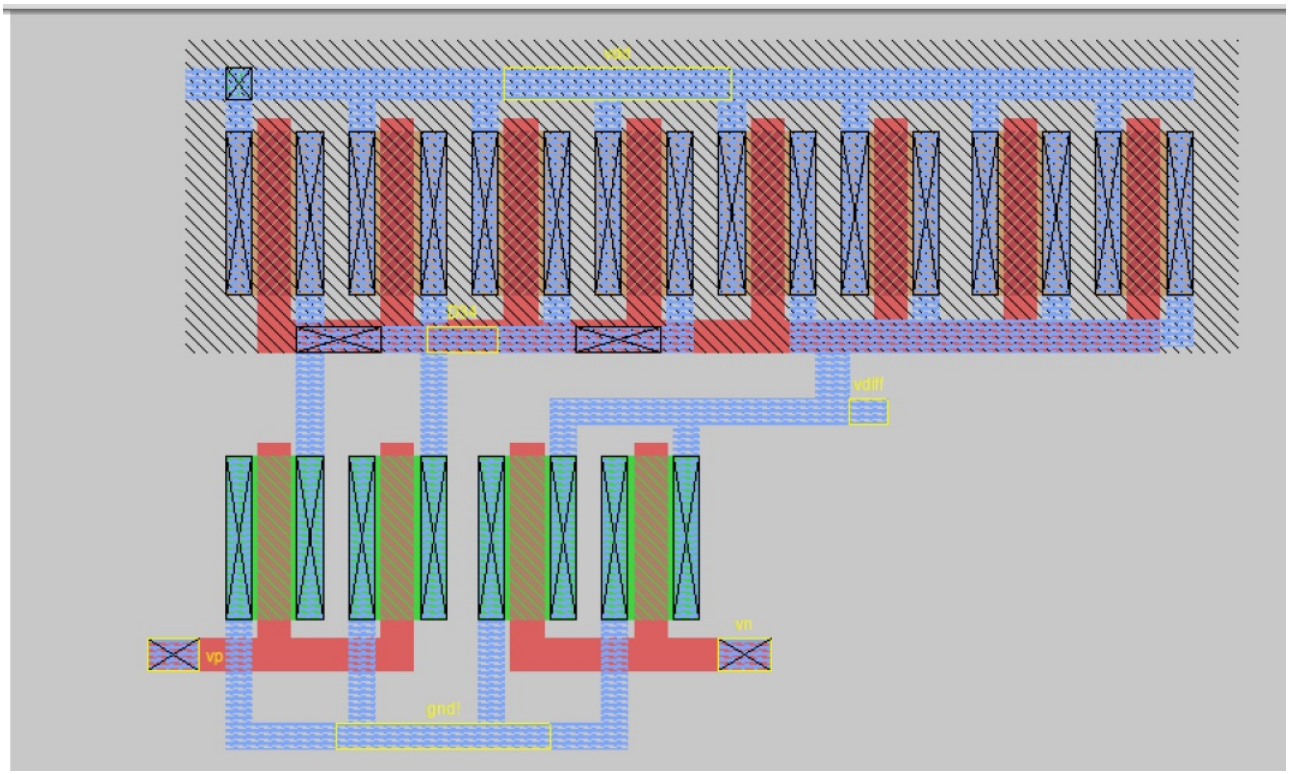

Figure 7: Lay out of Common Source amplifier

Conclusion

In this article Common source amplifier is analized and how to design CS amplifier with active load for a given specification is elaborated with an example. The designed amplifier is simulated using LT spice and results are verified.

Reference

1. Sedra ans Smith, "Microelectronic Circuits", Fifth edition, Oxford University press.