Design of MOS Cascode Amplifier using free and open source EDA tools

Guru prasad
Assistant Professor, MIT Manipal

Abstract

This article describes the analysis of Cascode amplifier and design it for given specifications. The design is simulated using SPICE tools and robustness is verified by Monte-Carlo simulations. Finally the design is laid out in 180 nm CMOS technology. This paper also demonstrates the use of free or open source software tools for electronic design automation and general purpose applications like word processing, data processing, data plotting and graphics editing etc.

Introduction

There are two main objectives of this article namely,

1. Analysis and Design of Cascode amplifier.
2. Promote the use of free and open source software tools.

Amplifiers are the basic building blocks of analog circuit system. There are many topologies available for different constraints and needs. However common source, common gate and common drain are the fundamental configurations, cascading them in different manner, many topologies can be derived.

Common source is basically a voltage controlled current source which provides both current and voltage amplifications with the change in phase. One of the demerits is the gain-bandwidth product is constant. i.e if gain becomes more, bandwidth is degraded due to miller effect. Whereas Common gate is current controlled current source which provides only voltage gain without change in phase. Since miller effect is absent in it, the bandwidth is not degraded by the increase in gain. It also has one demerit that its input impedance is less hence voltage signal experiences significant loss before reaching the amplifier.

What if there is a configuration which takes the merits of both common gate and source and rejects the demerits present in them. Since common gate is current controlled device, it expects a current source not voltage but common source is voltage controlled current source so if one feeds a voltage signal to a common source and its output is then fed to a common gate amplifier, the above mentioned desired configuration can be achieved. Th configuration is known as "cascode", cascade of common source and common gate. Figure 1 shows the Cascode amplifier structure.

In the figure M_1 is common source amplifier, M_2 is common gate amplifier and M_3 is active load. Figure 2 shows the small signal equivalent circuit.

Following conventions are used in the circuit analysis.

g_{mn} is transconductance of nth MOSFET.
S_n is dimension of of nth MOSFET.

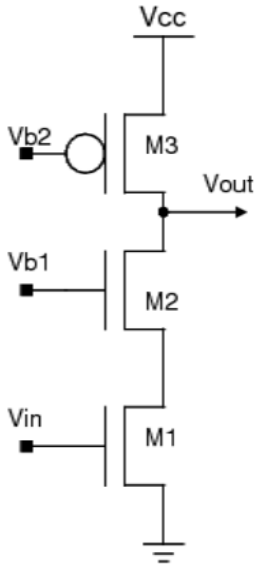

Figure 1: Structure of Cascode Amplifier

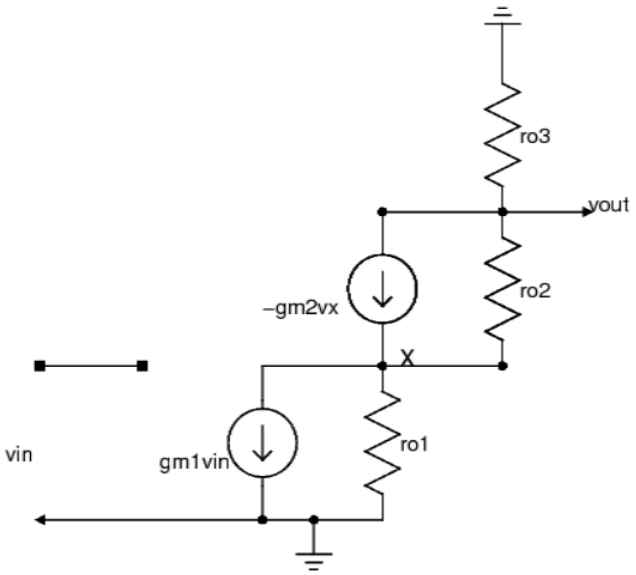

Figure 2: Small signal model of Cascode Amplifier

KP_n is $\mu_n C_{ox}$ of of nth MOSFET.
r_{on} is output resistance of nth MOSFET.
C_{GSn} is gate source capacitance of nth MOSFET.
C_{GDn} is gate drain capacitance of nth MOSFET.
C_{DBn} is drain bulk capacitance of nth MOSFET.
λ_n is channel length modulation of nth MOSFET.

$$Gain = \frac{vout}{vx} * \frac{vx}{vin}$$
$$= g_{m2}[r_{o3}||r_{o2}(1 + g_{m2}r_{o1})] * -g_{m1}[r_{o1}||1/g_{m2}]$$

if $g_{m2} = g_{m1}$ and $r_{o3} << r_{o2}(1 + g_{m2}r_{o1})]$ then

$$Gain \approx -g_{m2}r_{o3}$$

figure 3 shows high frequency model of Cascode amplifier. C_{GD1} is the only

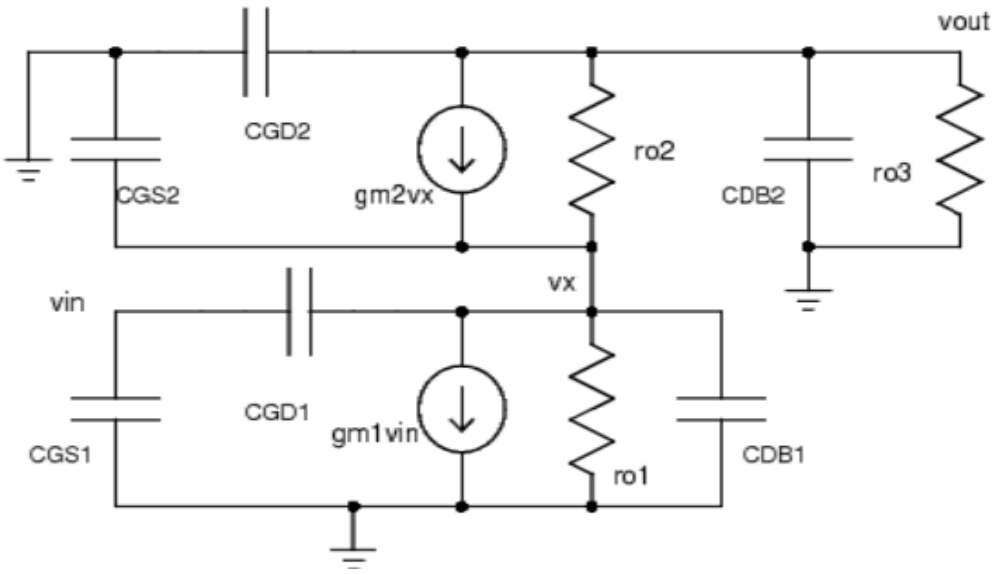

Figure 3: High frequency model of Cascode Amplifier

floating capacitor but since gain in first stage is almost equal to one $[g_{m1}/g_{m2}]$, miller multiplication is absent.

Circuit has three capacitors namely,

$$C_1 = C_{GS1} + [1 + C_{GD1}]$$

$$C_2 = C_{DB1} + C_{GS2} + [1 + C_{GD1}]$$

$$C_3 = C_{DB2} + C_{GD2} + C_L$$

Three poles can be determined as below

$$P_1 = C_1 * R_{signal}$$

$$P_2 = C_2 * 1/g_{m2}$$

$$P_3 = C_3 * r_{o3}$$

Among three P_3 is a dominant pole and decides the bandwidth of amplifier. It is evident that bandwidth is not dependent on gain of the amplifier.

Design of Cascode Amplifier

As an illustration purpose a design example is shown below. A cascode amplifier is designed for following specifications

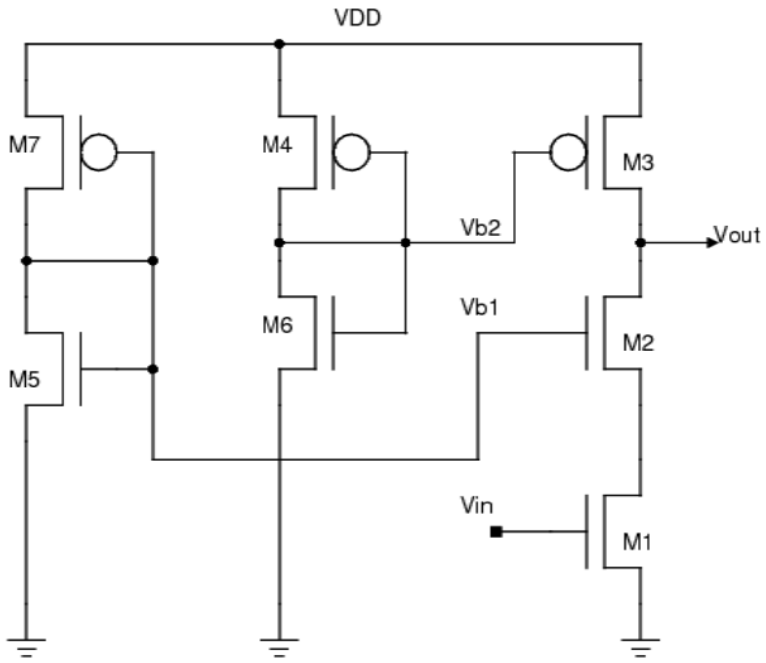

Figure 4: Complete circuit diagram of Cascode Amplifier

Table 1: Design Specification

Parameter	Value
Technology	180 nm
V_{DD}	1.8V
Gain	50
C_L	10pF
Power	<0.2mW
$V_{out,max}$	1.5V
$V_{out,min}$	0.6V
Slew Rate	$5V/\mu s$

Figure 4. shows the complete circuit diagram of cascode amplifier. [Allen and Hollberg(2008)]

1. Given power budget is <0.2mW and slew rate is $5V/\mu s$.

$$I_{dc} = Slewrate * C_L = 25\mu A$$

   Circuit has three branches hence total biasing current is $75\mu A$ and power consumption is 0.135 mW.

2. W/L ratio of M_3 is

$$S_3 = \frac{2I}{KP_3(V_{DD} - V_{out,max})^2} = 11$$

3. W/L ratio of M_1 is

$$S_1 = \frac{(Gain * \lambda)^2 I}{2KP_1} = 6$$

4. To find W/L ratio of M_2, the values of $V_{DS1,sat}$ must be known.

$$V_{DS1,sat} = \sqrt{\frac{2I}{KP_1S_1}} = 0.2V$$

5. From $V_{out,min}$ specification,

$$V_{DS2,sat} = 0.6 - V_{DS1,sat} = 0.4V$$

$$S_2 = \frac{2I}{KP_2(V_{DS2,sat})^2}$$

6. Gate source voltage of M_5 is

$$V_{GS5} = V_{DS1,sat} + V_{th} + \sqrt{\frac{2I}{KP_2S_2}} = 1V$$

$$S_5 = \frac{2I}{KP_5(V_{GS5} - V_{th})^2} = 1$$

7. W/L ratio of M_6 is same as M_3. Biasing current sources $25\mu A$ can be replaced by MOSFETs with suitable dimensions [From simulation tool by trial and error].

Simulation

LT-spice is a free simulation tool from Linear technology [Tech(2016)]. A brief user manual can be found from [Guruprasad(2016)]. In the present example, 180 nm CMOS BSIM 3V3 version SPICE parameters are assumed.

Initially operating point was calculated to verify whether all MOSFETs were in saturation region. Later input voltage was swept from 0V to 1.8V and output voltage was plotted as shown in Figure 5. To determine frequency response, an AC analysis was conducted. The amplifier exhibited a gain of 35 dB and -3dB bandwidth of 135 kHz as shown in Figure 6.

The design must be robust against device parameter variations. It can be tested by using Monte-Carlo simulation. *".Param, .mc function and .step"* commands together can do the above task. *.Param* command is used to set tolerance percentage, *.step* is used to conduct n number of iterations and *.mc* function varies device parameters randomly using Gaussian distribution with given tolerance percentage from nominal value. The reference [Jeff(2012)] can be used for detailed explanation. Figure 7 shows Monte-Carlo simulation of transfer gain of the designed cascode amplifier with 5% tolerance. It shows that probability of achieving gain=60 is more.

The circuit has been laid out in 180 nm CMOS technology using MAGIC VLSI layout tool [Tim(2016)] as shown in Figure 8. MAGIC VLSI is a open source layout tool which has built in MOSIS PDKs. It is very easy to use and has on-line DRC facility.

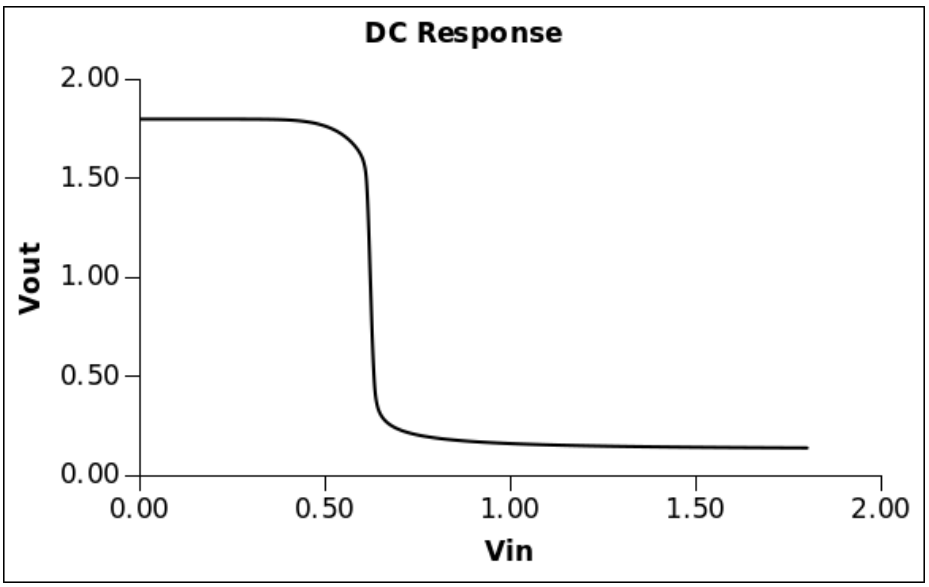

Figure 5: DC response of Cascode Amplifier

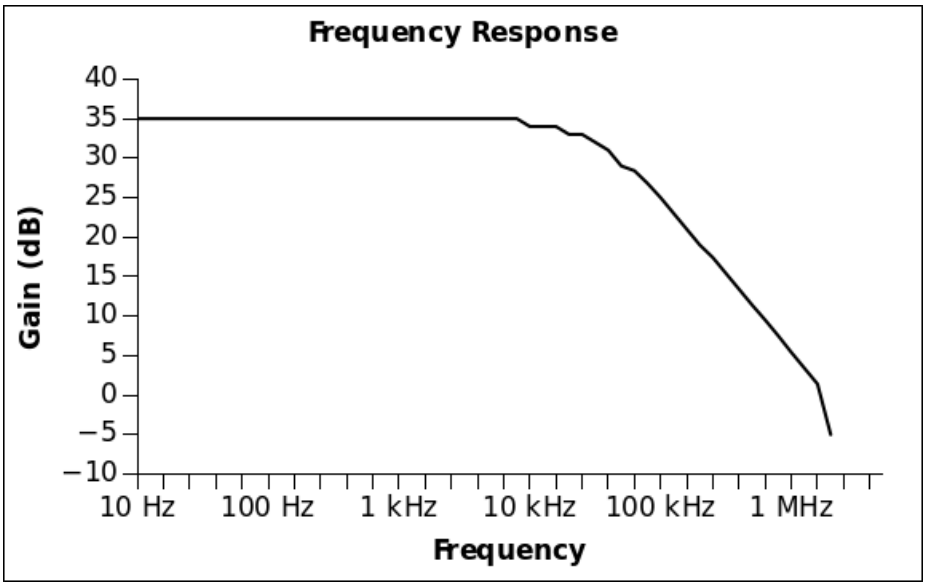

Figure 6: Frequency Response of Cascode Amplifier

Open Source / free software tools

For this article I have used only open source/free software tools listed below-

1. Lubuntu OS [Canonical(2016)]
2. Latex tool [Texmaker and Texlive] for word processing [xm1 Math(2016)]
3. Gnumeric for plotting data and Monte-Carlo histogram plot [GNU(2016)]
4. gschem for drawing schematic circuit diagrams [gEDA project(2016)]
5. LT-spice for simulation
6. MAGIC VLSI tool for layout
7. Shutter for screen shot [It is like "snipping tool" in windows][Kemper(2016)]

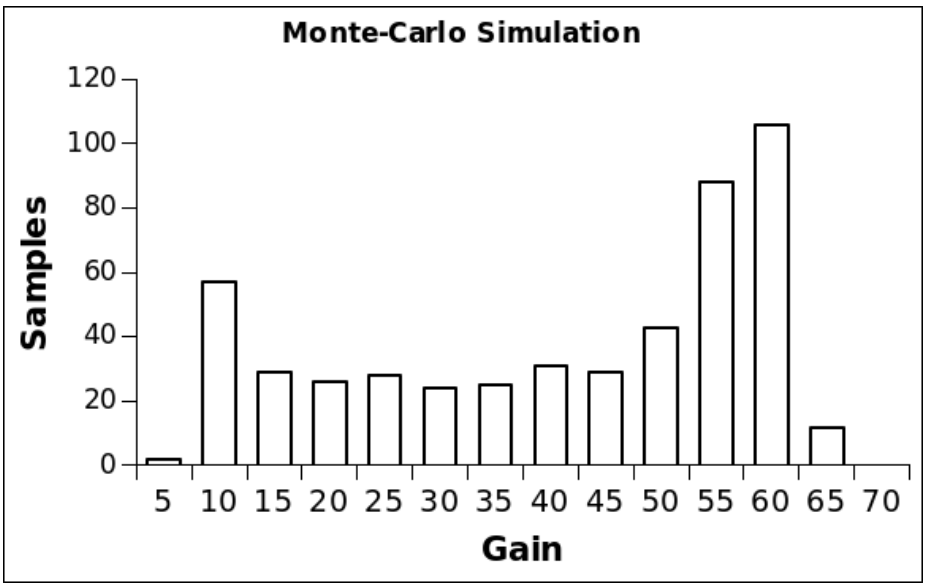

Figure 7: Monte-Carlo simulation result

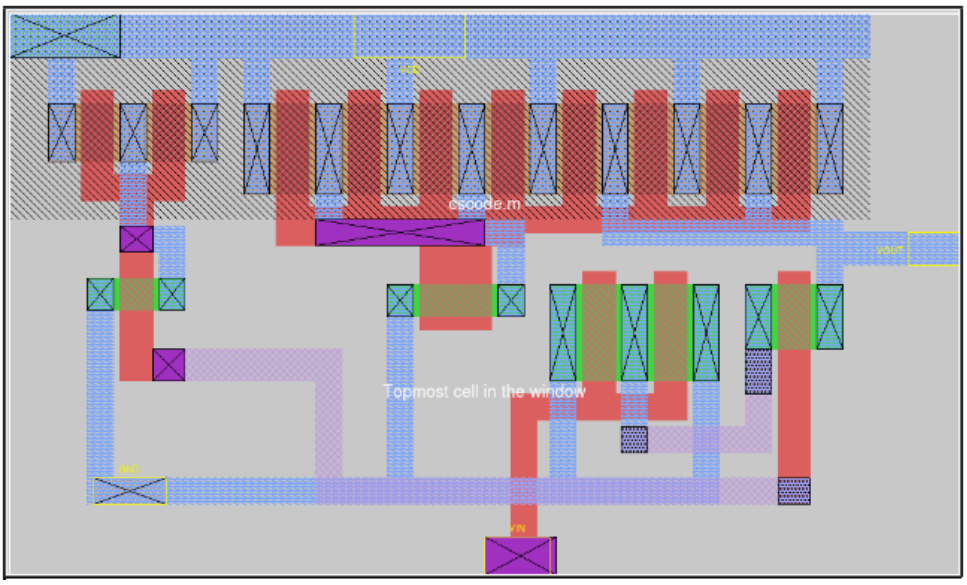

Figure 8: Layout of Cascode amplifier

8. mtPaint for graphics editing [Tyler(2016)]

Lubuntu is a light weight version of Ubuntu and a out of box Linux operating system. It takes only 20 minutes to install the entire OS. It is highly user friendly. Regarding the *Latex* tool, it is a complete word processor with professional quality output. One has to use it to feel its real power. *gschem* is part of gEDA tool and highly customizable. we can draw publication quality circuit diagrams using this. Like LTspice, there are other simulation tools, one can try like NGspice, Spice-OPUS, gnucap. Similarly for layout, one can use Electric VLSI, GLADE or layout editor. Totally I would like to say when there are plenty of open and free softwares available, why one has to always depend on propitiatory tools. Use open and free softwares and promote "open culture".

Conclusion

In this article an effort has been made to explain the analysis and design of Cascode amplifier. The design has been verified by simulation tool and laid out in 180 nm CMOS technology. The article also has demonstrated the use of free and open source software tools for electronic design automation and general purpose applications.

References

[Allen and Hollberg(2008)] Phillip E Allen and Douglas R Hollberg. Cmos analog circuit design textbook, 2008.

[Canonical(2016)] Canonical. lubuntu 16.04, December 2016. URL http://lubuntu.net/.

[gEDA project(2016)] gEDA project. Ltspice iv, December 2016. URL http://wiki.geda-project.org/geda:gaf.

[GNU(2016)] GNU. Gnumeric: Free, fast, accurate -pick any three!, December 2016. URL http://www.gnumeric.org/.

[Guruprasad(2016)] Guruprasad. Circuit simulation examples using ltspice, 2016.

[Jeff(2012)] Jeff. Monte carlo and worst-case circuit analysis using ltspice, 2012. URL http://k6jca.blogspot.in/2012/07/monte-carlo-and-worst-case-circuit.html.

[Kemper(2016)] Mario Kemper. Shutter: Screenshot tool, December 2016. URL http://shutter-project.org/.

[Tech(2016)] Linear Tech. Ltspice iv, December 2016. URL http://www.linear.com/designtools/software/.

[Tim(2016)] Tim. Magic vlsi layout tool, December 2016. URL http://opencircuitdesign.com/magic/.

[Tyler(2016)] Mark Tyler. mtpaint, December 2016. URL http://mtpaint.sourceforge.net/.

[xm1 Math(2016)] xm1 Math. Texmaker the universal latex editor, December 2016. URL http://www.xm1math.net/texmaker/.