Analysis and Design of MOS Differential Amplifier

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Guru Prasad
Manipal University
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Analysis and Design of MOS Differential Amplifier

Guru Prasad
Asst.Professor, MIT Manipal

Abstract

This article explains structure and analysis of MOS Differential amplifier and how to design it for a given specification. An example is taken to illustrate the design procedure and simulated using NG spice tool. Finally design is laid out using MAGIC VLSI tool.

Introduction

Differential amplifier forms the first stage in operational amplifier. It's function is to amplify only the difference between the two signals and reject any common between them. Figure 1 shows typical structure of active load MOS differential amplifier [1].

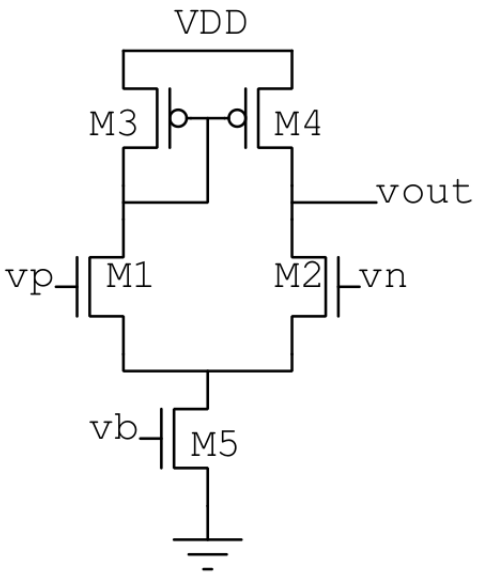

Figure 1: Typical structure of Differential amplifier

Signals vp and vn can be written as

$$vp = \frac{vp + vn}{2} + \frac{vp - vn}{2}$$

$$vn = \frac{vp + vn}{2} - \frac{vp - vn}{2}$$

if

$$vicm = \frac{vp + vn}{2} \qquad vd = \frac{vp - vn}{2}$$

$$vp = vicm + vd \qquad vn = vicm - vd$$

Analysis of Differential amplifier

Differential Gain

To analyze the differential amplifier, we have to consider differential inputs(vd) and common mode inputs (vicm) separately. Figure 2 shows the small signal circuit of differential amplifier for differential signals. The node where sources of M_1 and M_2 are connected acts as ground for differential signals [2].

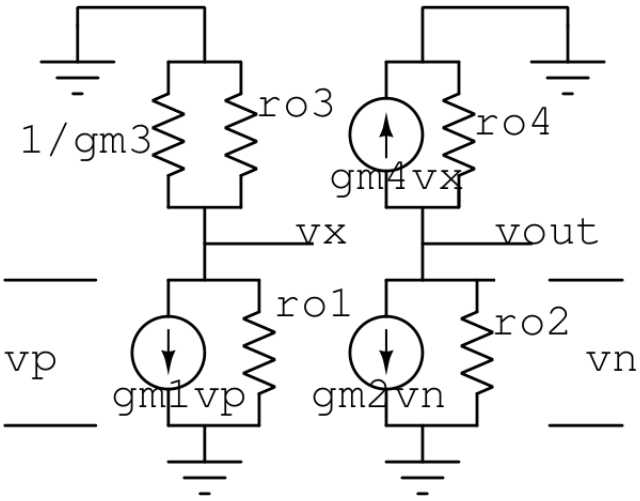

Figure 2: Small signal network of Differential amplifier for differential signals

In the Figure vp=vd and vn=-vd

$$vx = -gm1 * vd * (ro1||ro3||\frac{1}{gm3}) \approx -gm1vd * \frac{1}{gm3}$$

$$vout = -(r02||ro4)(gm4vx - gm2vd) = (ro2||ro4)vd(\frac{gm4gm1}{gm3} + gm2)$$

gm4=gm3 and gm1=gm2=gm then

$$vout = 2gmvd(r02||ro4)$$

$$vout = 2gm\frac{vp - vn}{2}(ro2||ro4)$$

$$Differnial\ \ Gain = \frac{vout}{vp - vn} = gm(ro2||ro4)$$

Common mode gain

Figure 3 shows the small signal network of differential amplifier for common mode signal[2]. In the figure ro5 is the output resistance of current source transistor M_5. For analysis purpose it is split into two equal parallel resistors 2ro5.

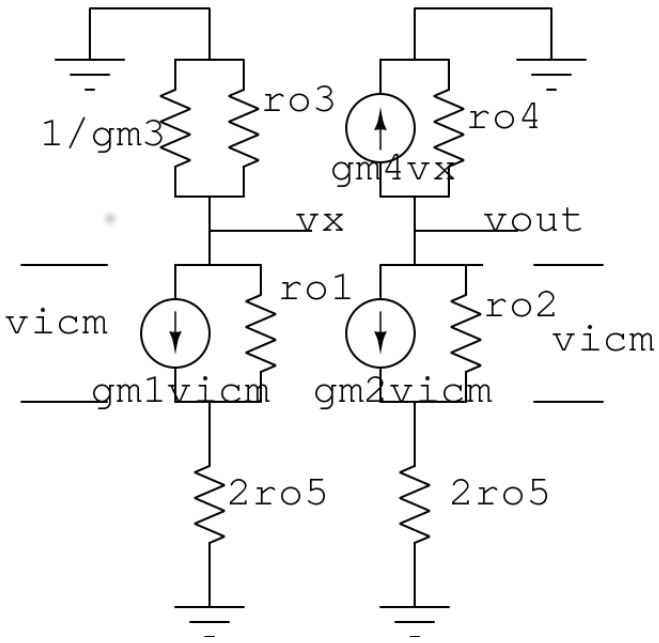

Figure 3: Small signal network of Differential amplifier for common mode signals

$$vx = -\frac{gm1(\frac{1}{gm3}||ro3) * vicm}{1 + 2gm1ro5} \approx -\frac{\frac{1}{gm3}||ro3 * vicm}{2ro5}$$

Due to source degeneration, the value of ro1 and ro2 resistors increases hence they are assumed as open circuit.

$$vout = -[(-\frac{\frac{1}{gm3}||ro3 * vicm}{2ro5} * gm4) + (\frac{vicm}{2ro5})] * ro4$$

$$vout = vicm[(\frac{\frac{ro3}{1+gm3ro3}}{2ro5} * gm4) - (\frac{1}{2ro5})] * ro4$$

$$\approx vicm * ro4[\frac{ro3gm4 - 1 - ro3gm3}{(1 + gm3ro3)2ro5}]$$

if gm3=gm4, ro3=ro4 and 1+gm3ro3=gm3ro3

$$vout = -vicm\frac{1}{2gm3ro5}$$

$$Commonmode\ \ gain = -\frac{1}{2gm3ro5}$$

CMRR

Common Mode Rejection Ratio [CMMR] is the ratio of differential gain to common mode gain. It is measure of how well a differential amplifier rejects the common mode signal hence considered to be a major performance parameter.

CMRR of above differential amplifier is give by

$$|CMRR| = \frac{gm(ro2||ro4)}{2gm3ro5^{-1}} = 2gm1 * gm3 * ro5(ro2||ro4)$$

Frequency Response

The simplified small signal circuit of differential amplifier is shown Figure 4 [2]. The circuit has two capacitances C_m and C_L. C_m is mainly formed by C_{gs3} and C_{gs4} but also includes C_{gd1},C_{db1} and C_{db3}.

$$C_m = C_{gd1} + C_{db1} + C_{db3} + C_{gs3} + C_{gs4}$$

Capacitance C_L includes C_{gd2}, C_{db2}, C_{db4} and C_{gd4}.

$$C_L = C_{gd2} + C_{db2} + C_{db4} + C_{gd4}$$

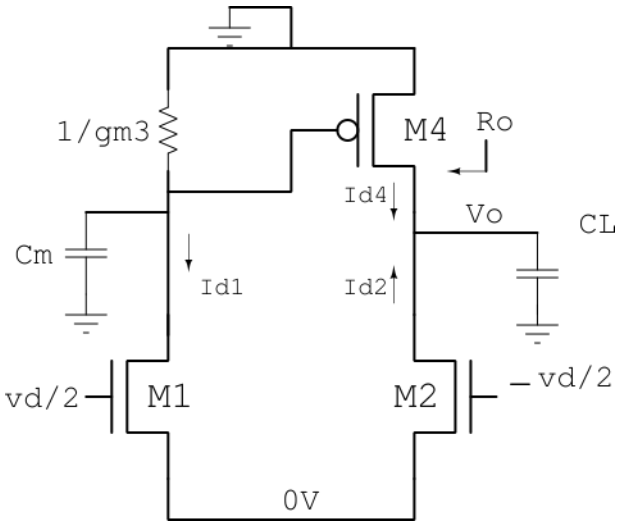

Figure 4: Simplified Small signal network of Differential amplifier

These two capacitances primarily determine the frequency response of differential amplifier. The transfer function of differential amplifier is given by

$$V_o = (Id4 + Id2)\frac{1}{\frac{1}{Ro} + sC_L}$$

$$= gmRo(\frac{Vd}{2})[1 + \frac{1}{1 + s\frac{Cm}{gm3}}]\frac{1}{1 + sC_LRo}$$

$$A_d(s) = \frac{V_o}{V_d} = (gmRo)(\frac{1}{1 + sC_LRo})(\frac{1 + s\frac{Cm}{2gm3}}{1 + s\frac{Cm}{gm3}})$$

$gmRo$ indicates the DC gain. The poles and zeroes of the system is given by

$$f_{p1} = \frac{1}{2\pi C_L Ro}$$

$$f_{p2} = \frac{gm3}{2\pi Cm}$$

$$f_z = \frac{gm3}{2\pi Cm}$$

Since $C_L R_o >> \frac{C_m}{gm3}$, f_{p1} is the dominant pole and phase margin will be always greater then 45^0.

Input common mode range

Input common mode range [ICMR] is the range of input signal for which all the transistors are in saturation region. The overdrive voltage of M_5 and V_{th} of M_1 decides the minimum ICMR and overdrive voltage of M_3 and V_{th} of M_1 decides the maximum ICMR.

Slew rate

The slew rate of the differential amplifier depends on the tail current source and capacitance from the output node to ground. It is defined by the amount of current that can be sourced or sunk into the output capacitor. It is given by

$$Slew \;\; rate = I_{d5} * C_L$$

Design of Differential Amplifier

The specifications for the differential amplifier might consists of:

- Small signal gain (A_v)
- Frequency response for the given load capacitance (f_{-3dB})
- Input common mode range
- Slew rate for given load capacitance
- Power dissipation

The design of Differential amplifier is an iterative procedure and applications specific. However following steps can be followed in general[3].

1. Select I_5 based on slew rate specification.
2. To meet the given f_{-3dB} calculate the required R_o and modify the I_5
3. Select $(\frac{W}{L})_{3,4}$ to meet the upper ICMR.
4. Select $(\frac{W}{L})_{1,2}$ to attain the specified gain.
5. Select $(\frac{W}{L})_5$ to meet the lower ICMR.
6. Repeat te above steps if all design specifications are not met.

Design example

Problem Statement: Design of a differential amplifier in 800 nm technology for the following specifications-

Table 1: Design Specifications

Parameter	Value
A_v	40dB
SR	$10V/\mu s$
f_{-3dB}	200kHz
$ICMR_{min}$	1.5V
$ICMR_{max}$	4V
P_{diss}	2mW
C_L	5pF

Table 2 gives the technology parameters of 800 nm CMOS technology.

Table 2: 800 nm CMOS technology parameters

Parameter	Value
V_{DD}	5 V
λ_P	$0.05V^{-1}$
λ_N	$0.04V^{-1}$
V_{tn}	0.7V
V_{tp}	-0.7V
K_N	$110\mu A/V^2$
K_P	$50\mu A/V^2$

Solution:
Step 1: To meet the slew rate specification, choose $I_5 > 10 * 5\mu A = 50\mu A$
Step 2: $f_{-3dB} = 200kHz$ needs a R_o of $250k\Omega$ i.e.

$$R_o = \frac{2}{(\lambda_N + \lambda_P)I_5} \leq 250k\Omega$$

Modify the I_5 as $100\mu A$
Step 3: Maximum ICMR is 4 V

$$V_{SG3} = V_{DD} - V_{ICMR} + V_{tn} = 5 - 4 + 0.7 = 1.7$$

$$V_{SG3} = 1.7 = \sqrt{\frac{2 * 50\mu}{50\mu(W/L)_3}} + 0.7$$

$$(\frac{W}{L})_{3,4} = 2$$

Step 4: The required gain is 40 dB=100

$$100 = gm1Ro = \frac{gm1}{gds2 + gds4} = \frac{\sqrt{2 * 110\mu(W/L)_1}}{(0.04 + 0.05)\sqrt{50\mu}}$$

$$\frac{W}{L}_{1,2} \geq 19$$

$$Take \qquad \frac{W}{L}_{1,2} = 25$$

Step 5: Minimum ICMR is 1.5 V

$$V_{ds5} = V_{ICMR} - V_{gs1} = 1.5 - \sqrt{\frac{2 * 50\mu}{110\mu 25}} - 0.7 = 0.6V$$

$$(\frac{W}{L})_5 = \frac{2I_5}{K_N V_{ds5}^2} = 6$$

Step 6: Design biasing circuit.

V_{gs5} is calculated so as to have I_5 as $100\mu A$

$$100\mu = 1/2 * 110\mu(W/L)_5(V_{gs5} - 0.7)^2$$

$$V_{gs5} = 1.27V$$

Use M_6 and M_7 transistors to provide a biasing voltage of 1.27 V. If bias current taken as $225\mu A$ then size of M_6 is $(13/6)^{th}$ of M_5.

Then PMOS M_7 size is calculated as follow-

$$225\mu = 1/2 * 50\mu(W/L)_7(3.73 - 0.7)^2$$

$$(\frac{W}{L})_7 = 1$$

Figure 5 shows the designed Differential amplifier.

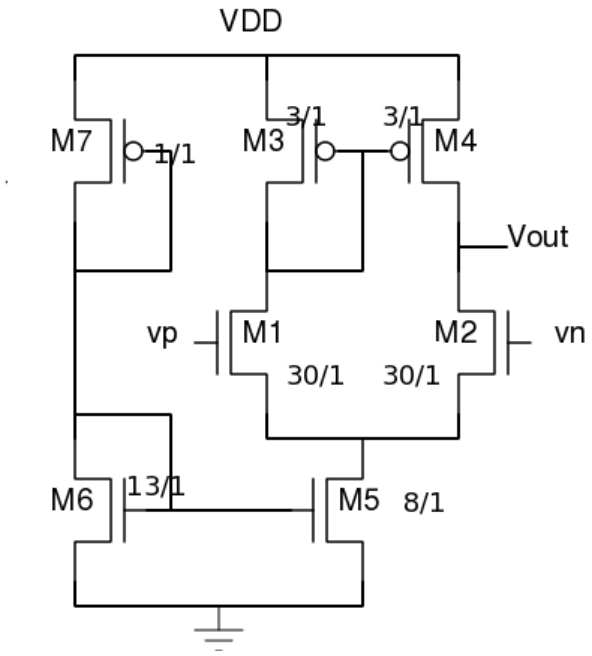

Figure 5: Designed Differential amplifier

Simulation

To verify the design, it was simulated using NG-Spice tool[4]. Figure 6 shows the net list of differential amplifier.

```
*Differential Amplifier in 800 nm Technology

VDD 7 0 5V
VP 1 0 dc 2.5v ac sin (0 1 2k)
VN 4 0 2.5V

M1 2 1 5 0 NMOS W=30U L=1U
M2 3 4 5 0 NMOS W=30U L=1U
M3 2 2 7 7 PMOS W=3U L=1U
M4 3 2 7 7 PMOS W=3U L=1U
M5 5 6 0 0 NMOS W=8U L=1U

M6 6 6 0 0 NMOS W=13U L=1U
M7 6 6 7 7 PMOS W=1U L=1U

CL 3 0 5p

.MODEL NMOS NMOS (LEVEL=1 VTO=0.7 KP=110U LAMBDA=0.04 CGSO = 2.20E-10
+CGDO= 2.20E-10 LD=0.016E-6 CGBO =700.0E-12 CJ = 770.0E-6 CJSW = 3.35744E-12
+MJ=0.5 MJSW=0.35 RD=40 RS=40 RSH=50 GAMMA=0.4 PHI=0.5)

.MODEL PMOS PMOS (LEVEL=1 VTO=-0.7 KP=50U LAMBDA=0.05 CGSO = 2.20E-10
+CGDO= 2.20E-10 LD=0.015E-6 CGBO =700.0E-12 CJ = 560.0E-6 CJSW = 3.5744E-12
+MJ=0.5 MJSW=0.35 RD=40 RS=40 RSH=50 GAMMA=0.5 PHI=0.5)

.OP
.END
```

Figure 6: Spice net-list of Differential amplifier

At first, DC operating point was found to check weather all MOSFETs are in saturation region. Then to determine the frequency response, a small signal was applied to non inverting terminal. Gain and phase response of differential amplifier were plotted in Figure 7 and Figure 8 respectively. The f_{-3dB} was approximately 200 kHz and gain found to be 40 dB as expected.

ICMR was measured by varying the voltage at the non inverting input from 0 V to 5V while differential amplifier was in voltage follower configuration. For the input range from 0.7 V to 4.4 V, differential amplifier was in linear region. This was much better than the expected.

The amplifier was designed for a slew rate of $10V/\mu s$ and after simulation same was obtained as shown in Figure 10. A pulse of 2V with $1\mu s$ transition time after a delay of $2\mu s$ was applied to differential amplifier in voltage follower configuration to test the slew rate.

Finally the design was laid out in 800 nm CMOS technology using MAGIC VLSI tool [5] as shown in Figure 11.

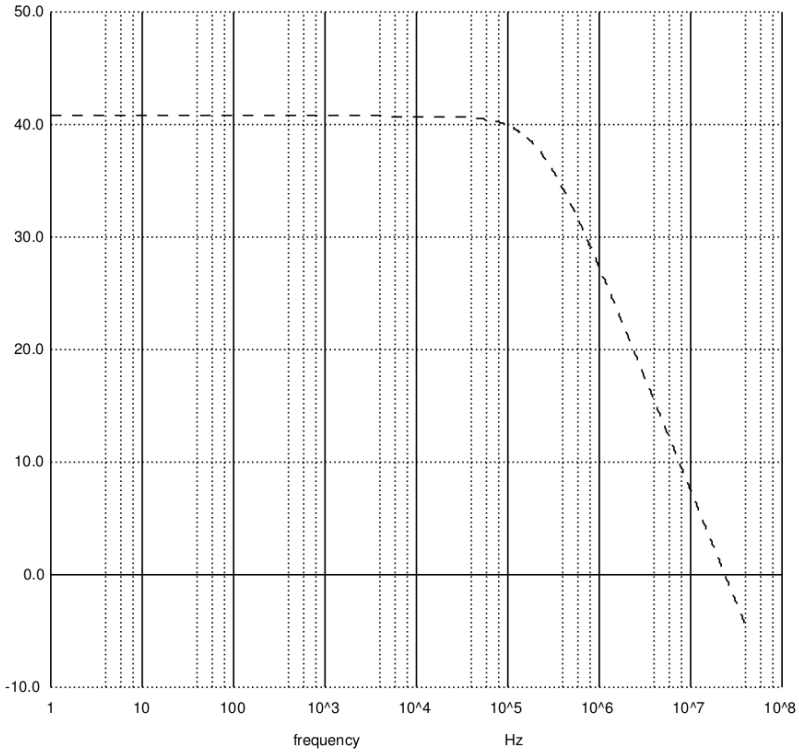

Figure 7: Gain response of Differential amplifier

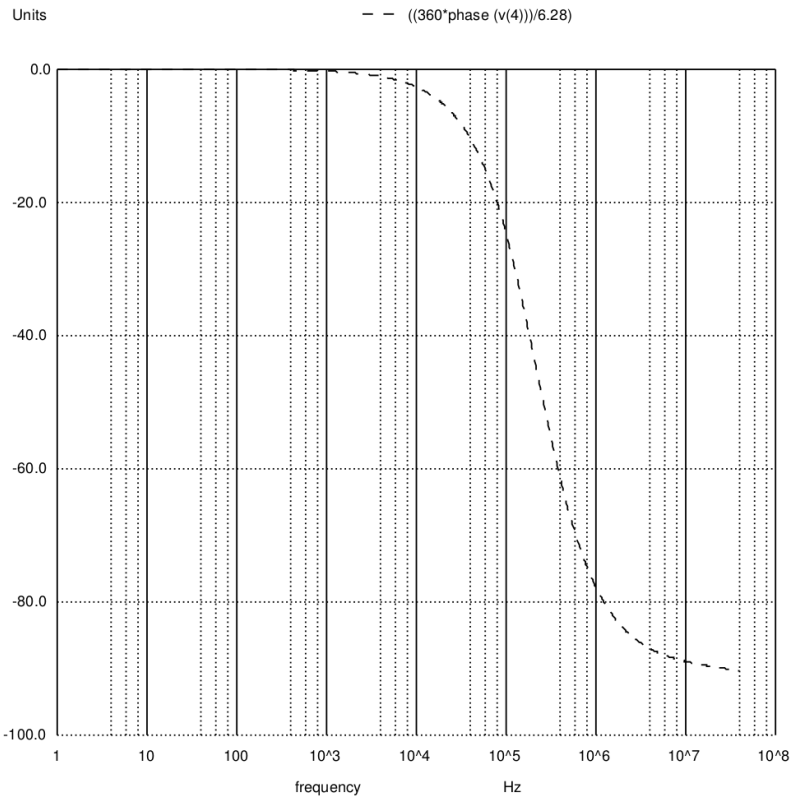

Figure 8: Phase response of Differential amplifier

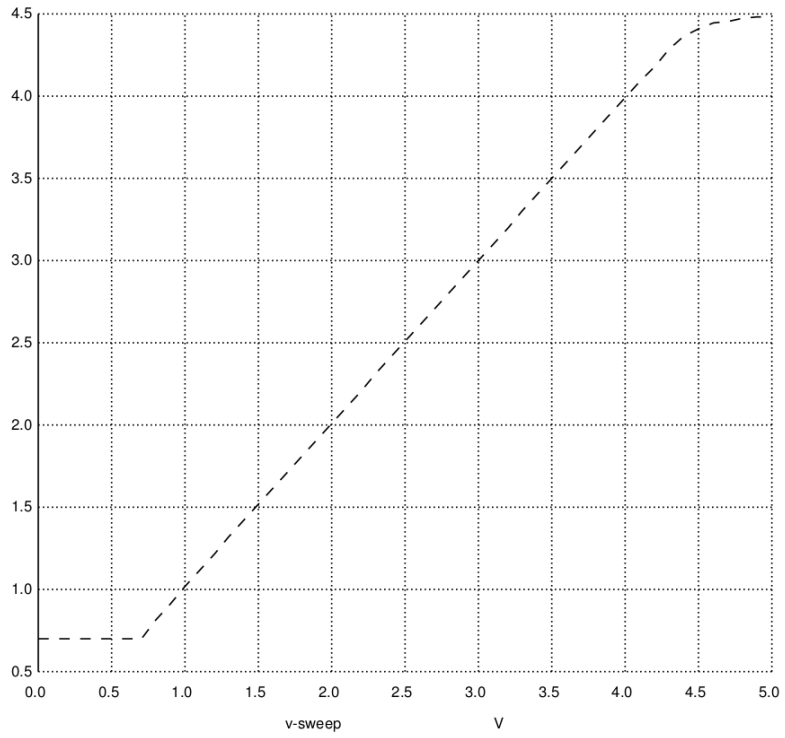

Figure 9: ICMR of Differential amplifier

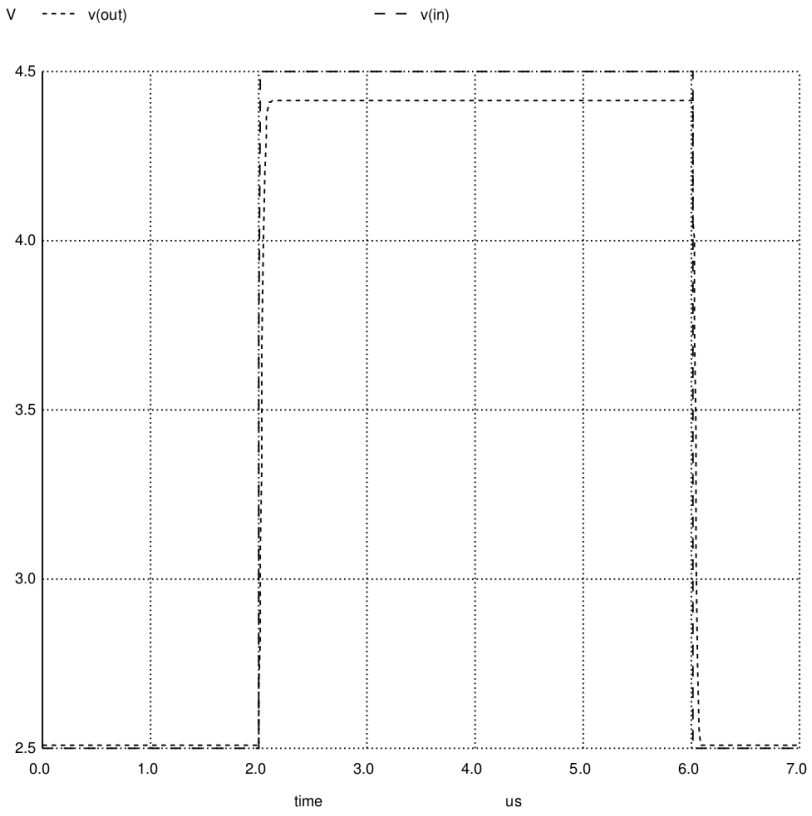

Figure 10: Slew rate of Differential amplifier

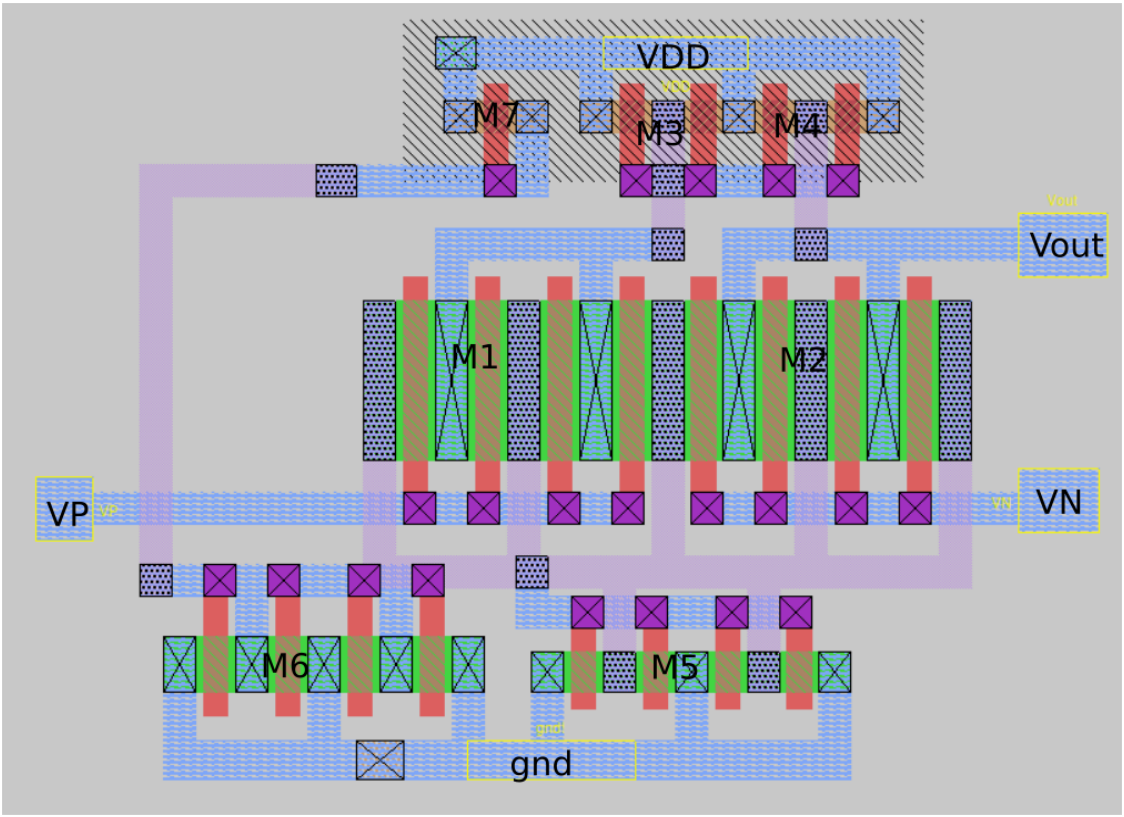

Figure 11: Lay out of Differential amplifier

Conclusion

In this article a MOS differential amplifier has been analized. The performance parameters like gain response, phase response, slew rate, ICMR have been explained. As an illustrative example,a MOS differential amplifier has been designed for the given specifications using 800 nm technology. The design has been verified using NG spice tool and laid out using MAGIC VLSI tool.

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