Operation Amplifier using Discrete Components

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Abstract

This article explains how to realize an operational amplifier using discrete components. General purpose BJT transistors, resistors, diode and capacitor are used to build op-amp. A three stage structure is assumed. Simulation results show that it provides a open loop gain of 130 dB with a phase margin of 70^0. The slew rate measured to be $2V/\mu s$.

Introduction

Operational amplifier is a very high gain amplifier typically used in a negative feedback system to achieve accurate gain. It's basic operation is listed as below-

1. Amplify only the voltage difference between two signals and reject any common between them.
2. Since not used with coupling capacitors, bring back the DC voltage level to origin to accommodate large output swing.
3. Since Operational amplifier is a voltage controlled voltage source it should offer low output impedance.

A typical op-amp should contain functional blocks as shown in Figure 1. The Differential amplifier, level shifter and buffer perform the jobs listed above respectively.

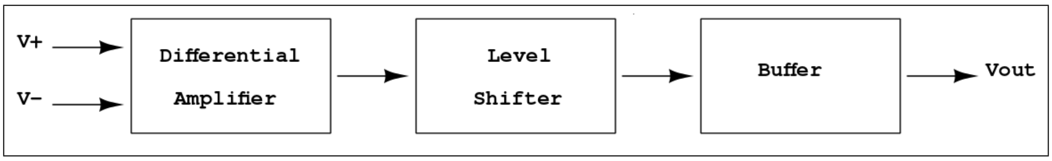

Figure 1: Op-amp Functional Block Diagram

Figure 2 shows the basic Differential amplifier. I_0 denotes the tail current source which decides the common mode rejection ratio of Op-amp. I_0 can be realized using transistor current mirror technique. The load resistors R_c can also be replaced by active load (pnp transistors).

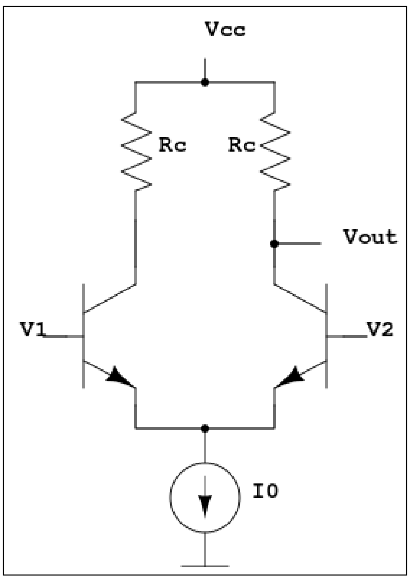

Figure 2: Differential amplifier

Figure 3 shows the basic level shifter which not only shifts the DC level but also provides small signal gain. I_0 is active load can be replaced by npn transistor.

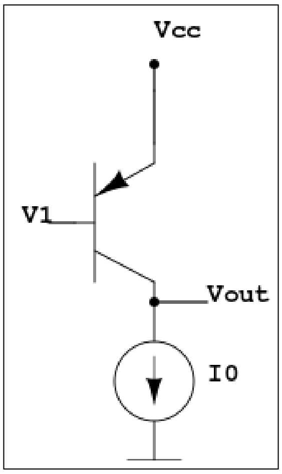

Figure 3: Level Shifter

Figure 4 shows a typical buffer which is a common collector stage. An active load npn transistor can replace I_0.

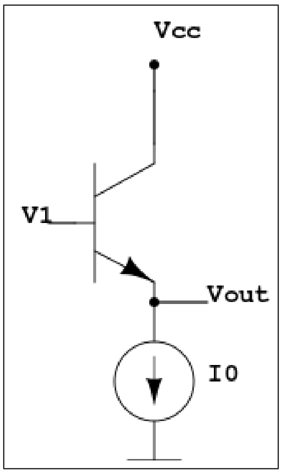

Figure 4: Buffer

Circuit Design

Figure 5 shows the complete circuit diagram of op-amp. List of components are

1. NPN transistor - 2N2222
2. PNP transistor - 2N3906
3. Silicon diode - 1N914
4. Resistors -10% tolerance - $20\Omega, 5.11k\Omega, 9.31k\Omega$
5. Capacitor - 400pF
6. Batteries - +5V and -5V

Since the bias current of last two stages is different from the differential amplifier stage [5 times more], Diode with resistors $5.11k\Omega$ and 20Ω are used to bias active load npn transistors in last two stages. If high frequency small signal model of op-amp is analyzed, it can be shown that the system has two dominant poles and makes it unstable. Hence a 400 pF miller capacitor is added in the circuit as shown in Figure 5 to make pole at the output of differential amplifier as single dominant pole and push the other pole beyond the unity gain bandwidth range.

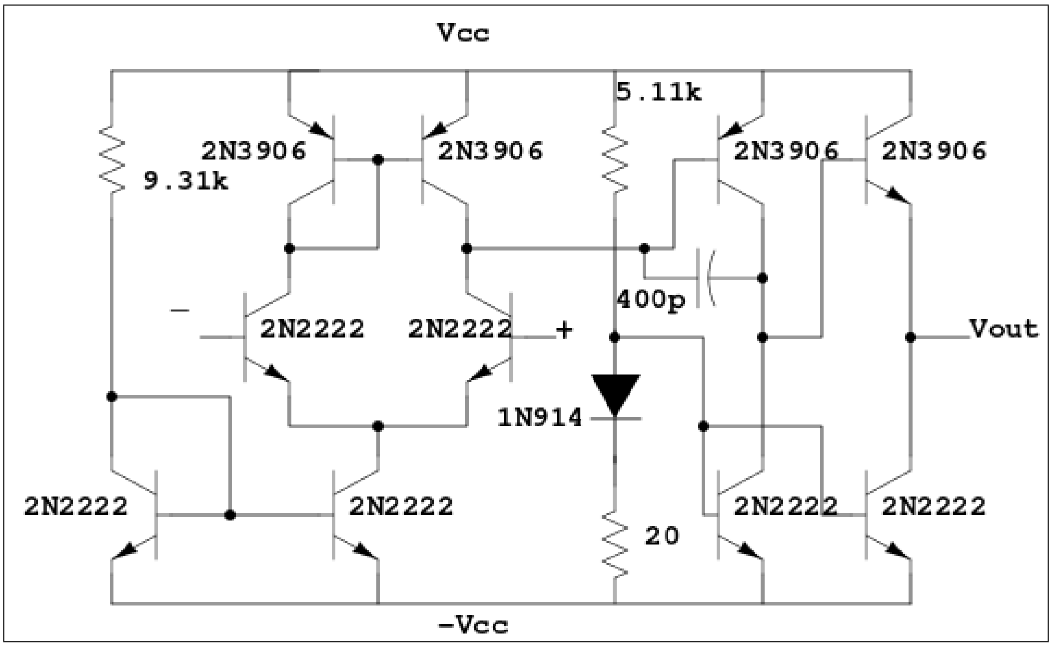

Figure 5: Complete Op-amp circuit diagram

The op-amp is simulated using Ng-spice and code is given below.

```
************************************************************
*Ng spice code for op-amp
V1 Vcc 0 5
V2 Vee 0 -5
V3 Vin 0 0
Q1 1 0 6 0 2N2222
Q2 3 0 6 0 2N2222
Q3 6 5 Vee 0 2N2222
Q4 5 5 Vee 0 2N2222
Q5 2 3 Vcc 0 2N3906
Q6 Vcc 2 Vout 0 2N2222
Q7 3 1 Vcc 0 2N3906
Q8 1 1 Vcc 0 2N3906
Q9 2 4 Vee 0 2N2222
Q10 Vout 4 Vee 0 2N2222
C1 2 3 400p
D1 4 7 1N914
R1 Vcc 5 9.31K
R2 Vcc 4 5.11K
R3 7 Vee 20

.model 2N2222 NPN(IS=1E-14 VAF=100 BF=200 IKF=0.3 XTB=1.5 BR=3 CJC=8E-12 CJE=25E-12
+TR=100E-9 TF=400E-12 ITF=1 VTF=2 XTF=3 RB=10 RC=.3 RE=.2 Vceo=30)
.model 2N3906 PNP(IS=1E-14 VAF=100 BF=200 IKF=0.4 XTB=1.5 BR=4 CJC=4.5E-12 CJE=E-11
+RB=20 RC=0.1 RE=0.1 TR=250E-9 TF=350E-12 ITF=1 VTF=2 XTF=3 Vceo=40)
.model 1N914 D(Is=2.52n Rs=.568 N=1.752 Cjo=4p M=.4 tt=20n Iave=200m Vpk=75)

.control
op
```

```
run
ac dec 100 10 30Meg
wrdata opamp (180/pi *phase(v(vout)))
*Use appropriate analysis commands here
.endc
.end
*********************************************************
```

Simulation Results

gnuplot is used to plot the simulation output. Figure 6 shows the simulation result of op amp. The op-amp performance is tabulated in Table 1.

Table 1: Op-amp performance

Parameter	**Obeserved Values**
Open loop Gain	130 dB and 1 MHz GBW
Phase Margin	70^0
Slew Rate	$+2V/\mu s$ and $-1V/\mu s$
Offset Voltage	100 mV
CMRR	110 dB
Temperature Response	Bias Current varies at $4mA/100^0C$

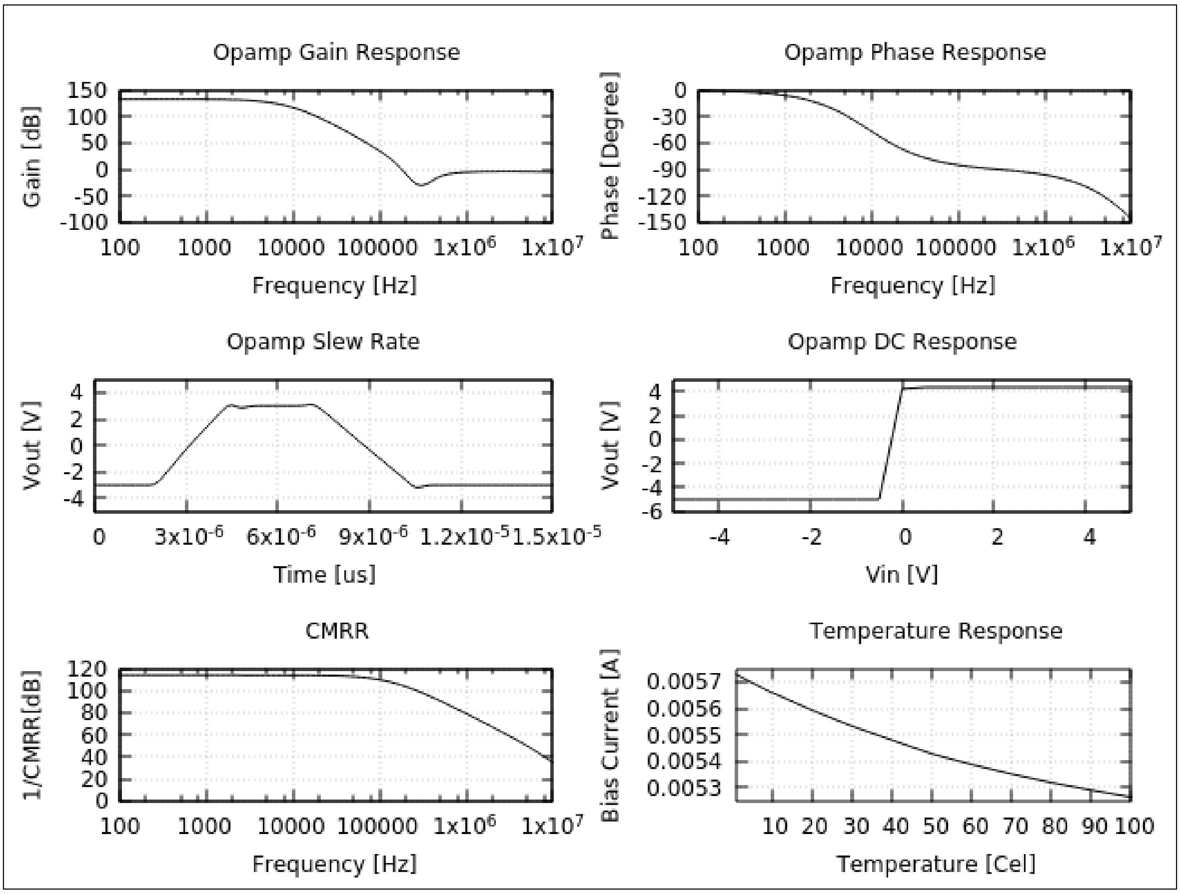

Figure 6: Simulation Results

gnuplot code for producing the above plot is given below
****

```
reset
unset key
set grid
set multiplot layout 3,2 rowsfirst scale 1,1

set xrange [100:10000000]
set xlabel "Frequency [Hz]"
set format x "
set xtics 10
set logscale x
set ylabel "Gain [dB]"
set title "Opamp Gain Response"
plot 'opamp.data' using 1:(20*log($2)) smooth bezier lc rgb 'black'

set xrange [100:10000000]
set xlabel "Frequency [Hz]"
set format x "
set xtics 10
set logscale x
set ytics 30
set ylabel "Phase [Degree]"
set title "Opamp Phase Response"
plot 'opamp1.data' using 1:2 smooth bezier lc rgb 'black'

set xrange [0:0.000015]
set xtics 0.000003
unset format xy
unset logscale x
set yrange [-5:5]
set ytics 2
set xlabel "Time [us]"
set ylabel "Vout [V]"
set title "Opamp Slew Rate"
plot 'opamp2.data' smooth bezier lc rgb 'black'

set xrange [-5:5]
set xtics 2
set yrange [-6:5]
set ytics 2
set xlabel "Vin [V]"
set ylabel "Vout [V]"
set title "Opamp DC Response"
plot 'opamp3.data' w l lc rgb 'black'

set xrange [100:10000000]
set xlabel "Frequency [Hz]"
set yrange [0:120]
set ytics 20
set format x "
set xtics 10
set logscale x
set ylabel "1/CMRR[dB]"
set title "CMRR"
```

```
plot 'opamp4.data' smooth bezier lc rgb 'black'

set xrange [1:100]
unset logscale x
unset format x
set xtics 10
set yrange [0.00525:0.00575]
set ytics 0.0001
set xlabel "Temperature [Cel]"
set ylabel "Bias Current [A]"
set title "Temperature Response"
plot 'opamp5.data' w l lc rgb 'black'
*******************************************************
```

All *.data files are generated by Ng-spice.

Conclusion

In this work an effort has been made to realize an op-amp using discrete BJTs and other components. Simulation results have shown that the performance of deigned op-amp is good. As a future work the same can be implemented on a Printed circuit board and physically be verified.

Reference

1. Sedra and Smith *Micro-Electronics Circuits* 5th Edition, Oxford Publisher, 2010.
2. Ngspice version 26-user manual.
3. Gnuplot version 5.0-user manual.
4. 2N2222, 2N3906 and 1N914 data sheets.