Design and Analysis of Super Source Follower

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Abstract

Source follower is a voltage controlled voltage source with unity voltage gain. It is usually used as buffer which offers lower output impedance and amplified current output. It's output resistance is approximately inversely proportional to the trans-conductance of MOSFET. Since trans-conductance of MOSFET is lower than BJT, the output resistance is not low as expected. Hence there is a need to modify the architecture of source follower. The present paper explains a solution which addresses the above issue.

Analysis of super source follower [SSF]

Source follower is also called as common drain amplifier as shown in Figure 1. The output voltage is equal to input voltage minus MOSFET threshold voltage. The small signal voltage gain and output impedance are given by equation (1) and (2) respectively [1, 2]. Assuming ideal current sources,

$$A_v = \frac{g_{m1} r_{o1}}{1 + g_{m1} r_{o1}} \tag{1}$$

$$R_o = \frac{1}{g_{m1}} || r_{o1} = \frac{1}{g_{m1} + \frac{1}{r_{o1}}} = \frac{V_{GS} - V_{th}}{2 I_D} \tag{2}$$

Where g_{mn} is the trans-conductance of n^{th} MOSFET and r_{on} is the output resistance of n^{th} MOSFET.

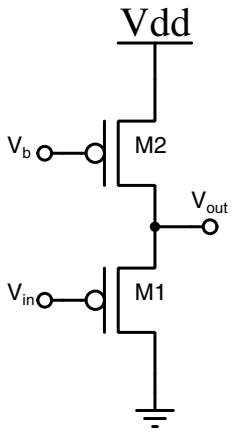

Figure 1: Circuit diagram of Source Follower

It is evident from equation (2) that output impedance is not very small. So one of the solutions would be to incorporate a negative feedback in the system. Figure 2 shows a modified architecture of source follower known as Super Source Follower [3, 4]. A common source amplifier is connected across the common drain stage. When current through M1 increases, the gate voltage of M2 also increases which in turn reduces V_{out} since M2 is in common source configuration. When V_{out} is reduced, the voltage difference between gate and source of M1 decreases there by reducing the the current though M1. This confirms the negative feedback action.

In the Figure 2, M3,M6 and M4,M5 form current mirror active load. Small signal equivalent circuit of SSF is shown in Figure 3. From KCL at output terminal,

$$\frac{V_{out}}{r_{o2}} + \frac{V_{out}}{r_{o3}} + g_{m2} V_2 + \frac{V_2}{r_{o4}} = 0$$

$$V_2 = -V_{out} \frac{\frac{1}{r_{o2}} + \frac{1}{r_{o3}}}{g_{m2} + \frac{1}{r_{o4}}} \tag{3}$$

From KCL at V_2,

$$\frac{V_2}{r_{o4}} + g_{m1}(V_{in} - V_{out}) + \frac{V_2 - V_{out}}{r_{o1}} = 0$$

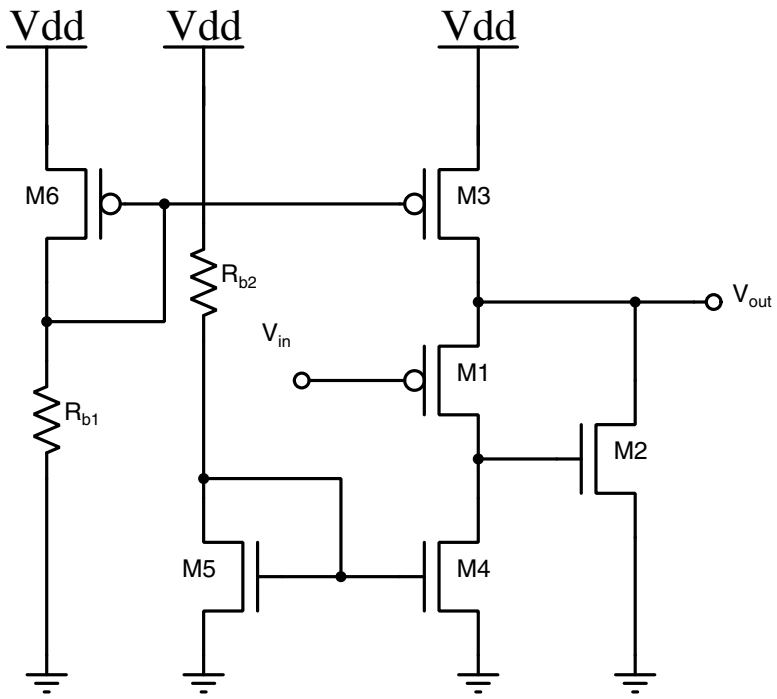

Figure 2: Circuit diagram of SSF

$$g_{m1}V_{in} = -V_2(\frac{1}{r_{o4}} + \frac{1}{r_{o1}}) + V_{out}(\frac{1}{r_{o1}} + g_{m1}) \tag{4}$$

Substituting for V_2 from (3) in (4),

$$g_{m1}V_{in} = V_{out}\frac{\frac{1}{r_{o2}} + \frac{1}{r_{o3}}}{g_{m2} + \frac{1}{r_{o4}}}(\frac{1}{r_{o4}} + \frac{1}{r_{o1}}) + V_{out}(\frac{1}{r_{o1}} + g_{m1})$$

Assuming ideal current sources,

$$g_{m1}V_{in} = V_{out}[\frac{1}{g_{m2}r_{o2}r_{o1}} + g_{m1} + \frac{1}{r_{o1}}]$$

$$A_v = \frac{g_{m1}r_{o1}}{\frac{1}{g_{m2}r_{o2}} + 1 + g_{m1}r_{o1}} \tag{5}$$

Voltage gain of SSF is smaller than the conventional source follower.

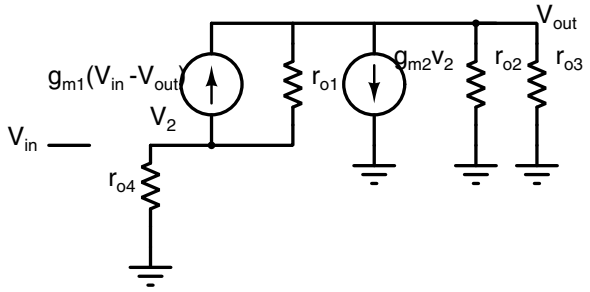

Figure 3: Small signal equivalent Circuit of SSF

The output impedance can be found by deactivating the input source and applying a test source at output and finding the ratio of voltage to current at output. Assuming ideal current sources,

$$I_x = \frac{V_x}{r_{o2}} + g_{m2}V_2 \tag{6}$$

From KCL at V_2,

$$g_{m1}V_x + \frac{V_2 - V_x}{r_{o1}} = 0$$

$$V_2 = V_x(1 + g_{m1}r_{o1}) \tag{7}$$

Substituting for V_2 in (6),

$$I_x = \frac{V_x}{r_{o2}} + g_{m2}V_x(1 + g_{m1}r_{o1})$$

$$R_o = \frac{V_x}{I_x} = \frac{1}{\frac{1}{r_{o2}} + g_{m2} + g_{m1}g_{m2}r_{o1}} \tag{8}$$

Comparing equation (8) and (2), it can be seen that the output resistance of SSF is significantly smaller than the output resistance of conventional source follower.

Results and Discussion

A SSF was designed using BSIM3 180 nm CMOS technology parameters and laid out using static Electric VLSI tool. Post layout simulation was carried out and the results were compared with pre-layout simulation. Table 1 shows the transistor sizes of MOSFETs used in SSF.

Table 1: Transistor size

Transistor	**Size**
M1	$\frac{100\mu m}{1\mu m}$
M2	$\frac{1\mu m}{1\mu m}$
M3	$\frac{40\mu m}{1\mu m}$
M4	$\frac{2\mu m}{1\mu m}$
M5	$\frac{1\mu m}{1\mu m}$
M6	$\frac{40\mu m}{1\mu m}$

Figure 4 show the voltage transfer characteristics curves SSF before and post layout. From 0V to 0.9V the output voltage follows input linearly. The AC response of SSF is shown in Figure 5. The measured voltage gain is 0.742. The output impedance of SSF is determined using SPICE simulation. Figure 6 shows that the output impedance of SSF is $4.1k\Omega$ before layout and $2.8k\Omega$ after layout. The layout of SSF is shown in Figure 7.

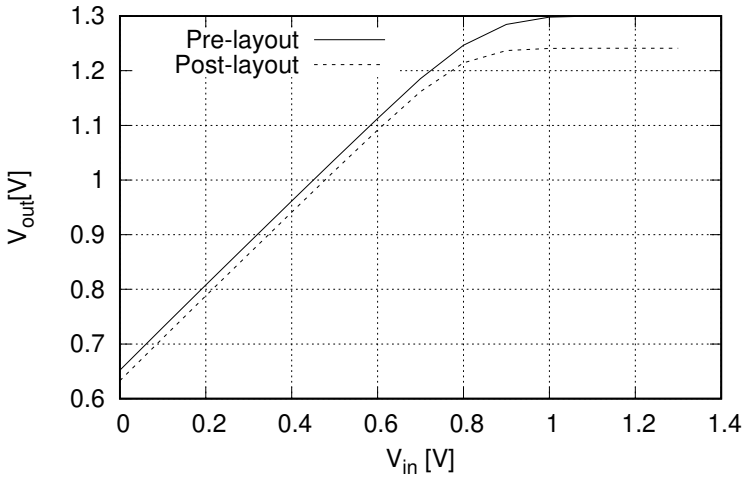

Figure 4: Voltage transfer characteristic of SSF

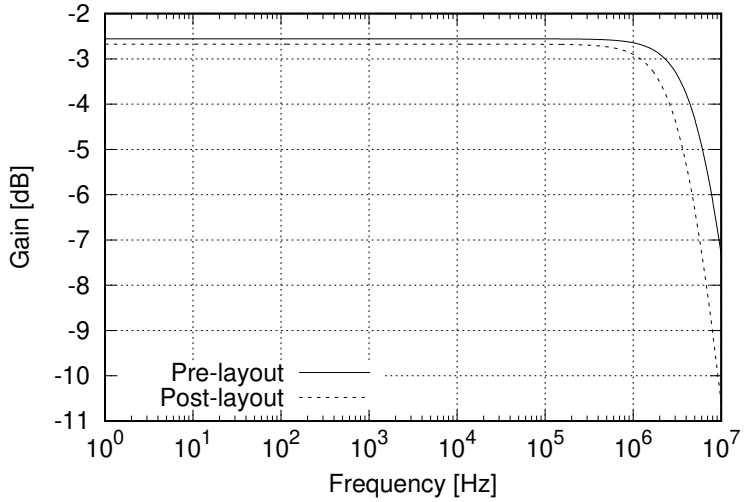

Figure 5: Frequency response of SSF

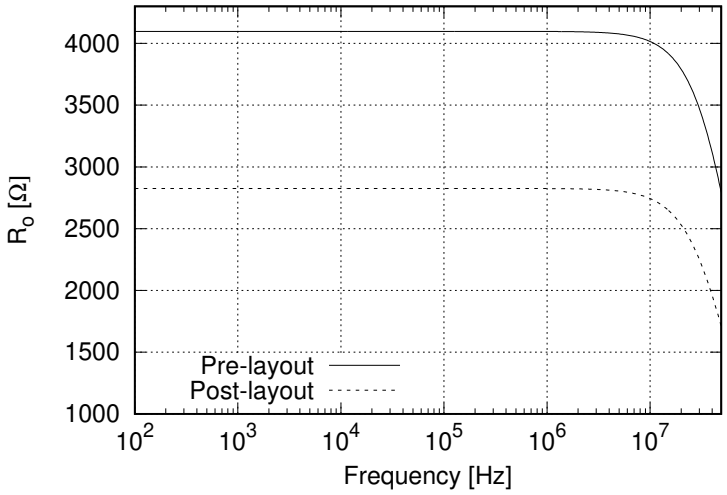

Figure 6: Output resistance of SSF

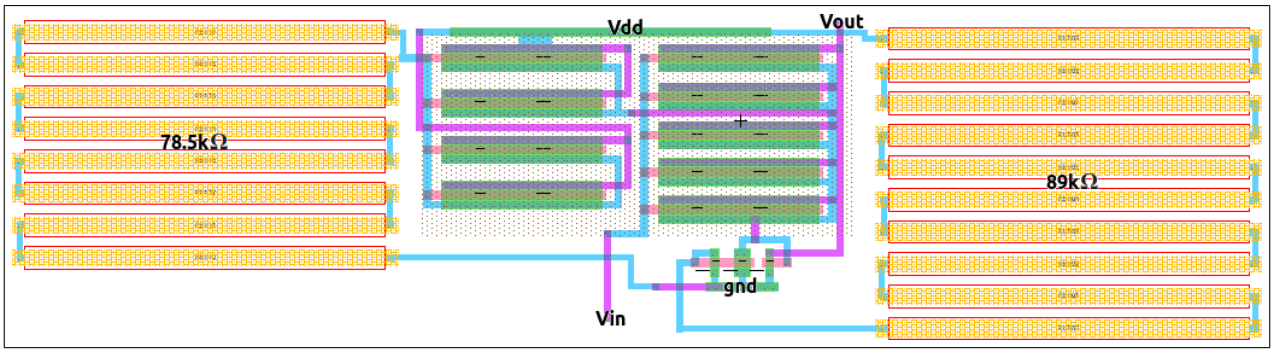

Figure 7: Layout of SSF

Conclusion

In the present paper, a super source follower is analyzed and its merits are explained. A SSF is designed and laid out using 180 nm CMOS technology. Post layout simulation results show that the performance of designed SSF match

with expected. The entire design and simulations have been carried out using open source EDA tools.

References

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