Guruprasad
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Education

Year	Degree	Institute
2021	Ph.D (Analog Circuits)	Manipal Institute of Technology, Manipal
2008	M.Tech (Digital Electronics & Communication)	NMAM Institute of Technology, Nitte
2006	B.E (Electronics & Communication)	SJCE, Mysore

Work Experience

- Junior Design Engineer at KarMic Design Private Limited, Manipal since November 11, 2024.
- Associate Professor with Department of Electronics & Communication Engineering, Shri Madhwa Vadiraja Institute of Technology, Bantakal from 01-09-2022 to 05-11-2024.
- Assistant Professor, senior scale with Department of Electronics & Communication, Manipal Institute of Technology, Manipal from 17-06-2008 to 30-08-2022.

Projects at KarMic

1. **BEANIE project - 1.8 V NMOS LDO block** (Technology - lbc10lv)
   - Assisted in modifying and designing the biasing circuit for the LDO.
   - Ran PVT and Monte Carlo simulations for the following tests and verified the results
     a. Biasing b. Line Regulation c. Load Regulation d. Stability e. PSSR f. Start-up Sequence g. Load Transient h. Wafer Burn-in test i. Aging Test
   - Conducted the above tests on block level where along with LDO, other connecting blocks like Power-on reset, Band-gap, Band-gap Resistor-Trimming, Ramp generator, A to D converter and capacitive loads were present.
   - Carried out resistor trimming simulation and passing the code values to achieve accurate reference voltage for the LDO
   - Assisted in post-layout simulations.
2. **Design and verification of MOS only voltage reference circuit** as part of training (Technology - lbc10lv) under the guidance of Mr. Raghavendra Hebbar and Mr. Jayasheel Shetty, Senior design Engineers.
   - Designed a 0.6 V voltage reference circuit. It used diode-connected MOSFETs operating in the subthreshold region to generate PTAT and CTAT currents.
   - The resistor trimming circuit was developed to remove the variations between the corners. I generated different codes across PVT corners and used in simulation.
   - Created test benches to carry out the following PVT and Monte Carlo simulations and verified the same
     a. Resistor Trimming b. DC biasing c. Temperature sweep d. Supply sweep e. Start-up transient f. PSRR g. Wafer Burn-in h. Aging
3. **Design and verification of PMOS LDO** as part of training (Technology - lbc10lv) under the guidance of Mr. Raghavendra Hebbar and Mr. Jayasheel Shetty, Senior design Engineers.
   - Designed a cap-less PMOS LDO with an output voltage of 1.8 V, 10 mA load, quiescent current of 10 μA and accuracy of less than 1%.
   - Before carrying out the simulations, the theoretical values of all the performance parameters were calculated using derived expressions.
   - Conducted PVT and Monte-Carlo simulations to verify all the performance parameters and compared with the theoretical values.
4. **Design and verification of CMOS Comparator** as part of training (Technology - lbc10lv) under the guidance of Mr. Raghavendra Hebbar and Mr. Jayasheel Shetty, Senior design Engineers.

- Designed a CMOS comparator with a supply voltage of 1.8 V, a hysteresis of 116 mV, quiescent current of 8 μA and propagation delay of under 30 ns.
- It had 5 stages, namely, Pre-amplifier, Latch, Post-Amplifier, Schmitt trigger and inverter.
- Five percentage of supply voltage variation, temperature variation from -45 °C to 175 °C and different process corners were considered.
- Carried out PVT and Monte-Carlo simulation for the following parameters
  a. Biasing b. Hysteresis c. AC analysis d. Transient analysis

5. **Chip level Testing of Z1338CMMB13B memory IC** (Technology - bcs13) with Vinay N D, Analog design Engineer, Texas Instruments Bangalore. Duration: 01-05-2025 to 20-05-2025
   - Investigated working flow of chip, functions of each I/O pins, architecture without datasheet.
   - Designed a testbench to test power-up sequence and IDDQ current across all PVT corners.
   - Determined the sequence of required signals for programming the memory bits and checked the programming currents to verify the same.
   - Designed a testbench to read the memory content of all the bits.
   - Designed a testbench for Margin testing which includes four types and current for each type was measured and verified.
   - Derived a testbench for bypass mode and determined the propagation delay of all the memory blocks across all the PVT corners.
   - Conducted external IREF current margin testing for each of the memory blocks.
6. **External IREF Margin testing of 13 NVM IPs** (Technology - lbc9, lbc10, lbc10mv, hpa9) with Vinay N D, Analog design Engineer, Texas Instruments Bangalore. Duration: 20-05-2025 to -2025
   - For each IP, studied the data sheet to the function of each pin and specifications.
   - Determined PS (Program Strength) value, program current, read current and voltage drop across the programming transistor.
   - Calculated PS value for post bake condition based on voltage drop across the programming transistor.
   - Modified the programming strength of two memory bits, one with post burn value and another one with post bake.
   - Designed a testbench to determine the post burn and post bake currents.
   - Ran a Monte-Carlo simulation for 36 corners (6 voltages at 6 different temperature) with following settings - Sample -1000, MCPD filter, Process variation : Gaussian – 4 sigma, Process Mismatch : Gaussian – 6 sigma
   - From the result, Calculated minimum post burn and bake currents for each voltage, at each temperature.
   - Plotted the linear graphs of Current vs Voltage at -40,25 and 125 degree celcius temperatures. Also fitted the linear equation for the same and listed slope and intercept.

Projects at Academic Institutions

1. **An Area Efficient LDO Regulator With Improved Transient Response for Hearing-aid Applications**
   - MOSIS CMOS 180 nm node
   - Tools used - Electric VLSI, NG-spice, Gnuplot, Xcircuit
   - Duration - Jan 2022 - Dec 2022
2. **Comparative analysis of PMOS and NMOS based linear regulators with similar power profile**
   - Output power of 18 mW. PMOS $\rightarrow$ VO = 1.6 V, IO =11.25 mA ; NMOS $\rightarrow$ VO = 1 V, IO =18 mA
   - Tools used - NG-spice, Gnuplot, Xcircuit
   - Duration - Jan 2023 - Nov 2023
3. **A Tutorial on Design of Datapath and Controller of an ALU in Verilog using Open Source EDA Tools**
   - Tools used - Icarus verilog, GTKwave
   - Duration - Sep 2022 - Nov 2022
4. **Design and Verification of Analog Integrated Circuits Using Free or Open source EDA Tools**
   - Design of a three stage CMOS Opamp in 180 nm MOSIS CMOS node
   - Tools used - gEDA-gschem, NG-spice, Electric VLSI, Gnuplot, Xcircuit
   - Duration - Sep 2018 - Jan 2019

5. **FPGA implementation of IIR filter using modified Booth multiplier**
   - Design of 16 bit floating point multiplier and other arithmetic circuits
   - Tools used - Xilinx, Modelsim
   - Duration - Oct 2007 - May 2008

Ph.D Thesis

Title: Investigation on performance improvement of LDO voltage regulator
This work was about designing a novel LDO regulator in 180 nm CMOS technology with output voltage 1 V and load current 100 mA with improved transient response. Dynamic and adaptive biasing techniques, source bulk modulation of pass transistor were used to enhance the performance. Also, a 0.6 V, MOS-based voltage reference was designed with a focus on improving the line regulation. Both circuits were laid out and post layout simulations were carried out to verify the performance.
Duration : April 2014 to November 2021.

Achievements

- Published six technical articles in international reputed peer reviewed journals.
- Presented five technical papers in IEEE international conferences.
- Topper in NPTEL course on *Power Management IC* from IIT Chennai in April 2022.